

Nascom RAM B 4Mhz / 48K Dynamic Memory Card

Constructional and Functional Specification

D O C U M E N T A T I O N

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NM Part No. 024-300

Issue 2

21/4/80



Nascom Microcomputers

NASCOM type B RAM board: PCB modification

On issue 3 board, immediately adjacent to LK2, there will be found a wide track running along the edge of the board at right angles to the edge connector.

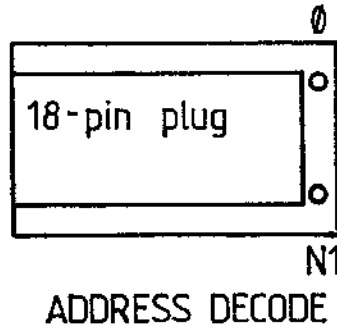
If only one through-plated hole is provided to connect the wide track to its counterpart on the other side of the board it is recommended that a piece of wire be soldered through the hole to provide greater current capacity.

S U B S T I T U T I O N

Type B Memory Board

In this kit the 20 pin header plug for SK1, the decoding linksocket, has been replaced with an 18 pin plug.

This plug should be wired in exactly the same way as the 20 pin plug, omitting connections to pins 1 (0000) and 20 (N1 M. EXT). The plug should be inserted in the 20 pin socket to make contact with pins 10 and 11 but not with pins 1 and 20.



If a NASCOM-1 system is in use, pin 20 may need to be wired; in this case, the plug should be used at the other end of the socket. The only case in which difficulty may arise is that in which a NASCOM-1 is being used in conjunction with 48K of memory on one board; if this circumstance arises please contact us and we will endeavour to assist.

We sincerely regret any inconvenience caused by this temporarily necessary substitution.



Nascom Microcomputers

18:07:80
ref: 024-300i2

B-type RAM board: documentation errata

- page 1-2 Under 'Circuit ref'
 for IC42 Read IC39 ✓
 for RP3 Read RP4
 for RP4 Read RP5
- page 1-5 fig. 3: write protect switch links
 for SW1 Read SW3
 for SW3 Read SW1
- page 1-6 para. 7: intergrated circuits: item (9)
 to 74LS74 ADD 'or 74S74'
- page 2-5 memory test object code
 address 0D0H
 for 3CH Read C3H
- the illustration of the display
 produced is not exactly as it would
 appear on the screen.
- page 3-4 the space allocated to the existing
 operating system should be ~~0000~~
 to 07FF.
- page 3-7 under '32K of Memory'
 for 0 & 2 Read 0 & 1
- under '48K of Memory'
 drawing: pin 18
 for B0 Read B1
- Circuit diagram 024-401 Cs 74, 75 and 76 should be .2u2 and
 not 4u7 as shown.

Please inform us if you detect any further errors in this or other documents; we are always grateful to know of them.

NASCOM Documentation Department

Introduction

The RAM B is a Dynamic random access memory board. The memory may be configured to have a memory capacity of 16k, 32K or 48K bytes of user RAM. This on-board memory expandability is made possible by population options of either eight, sixteen or twenty-four MK4116 (16,384x1 MOS dynamic RAM) memories. The RAM B provides options for positioning the decoded memory space to start on any 4K address boundary. The RAM B also includes logic for a "Page mode operation" which permits up to four, fully populated, RAM B boards to be used in one system (192K in total).

This Manual contains all the information necessary to build, test and use your 4Mhz - 48K Dynamic RAM card. A separate Manual has been produced to cover the additional construction and use of the Page mode and Write protect upgrade kit (part no 024-110).

Section number	Title	Page number
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SECTION 1

Construction

1. Do not begin construction now. Read through all the documentation at least twice before starting in order to ensure that no fundamental and expensive errors are made.
2. Do not leave the MK4116 Dynamic RAM integrated circuits out of their antistatic packing. (see Nascom 1 or 2 Manual for MOS handling instructions).
3. Keep the box in which the RAM card was delivered in case it should have to be returned for repair.
4. Do not attempt to use too large a soldering iron. Use an earthed 15 to 25 watt soldering iron equipped with a suitably small bit. Use the 22 Swg resin-cored solder supplied with the kit.
5. Fit all components in the board on the same side as the printed information.
6. Be certain to fit all integrated circuits and tantalum bead capacitors in the correct locations and the correct way round.
7. Be certain to connect the power supplies to the Bus the correct way round. (See Nasbus functional specification, part No. 003-310).
8. Do not attempt to remove or plug in, integrated circuits on the board, or perform any soldering while the power supply is switched on.
9. If any difficulty is experienced when plugging an IC into its socket do not use extreme force. If in doubt remove the IC; check that the pins are straight and parallel and start again. An IC insertion tool may be found useful. Note that all ICs are manufactured with the leads spread apart by a few degrees to suit mechanised handling equipment. They can be bent parallel with care using small pliers or one row at a time by pressing down sideways on a flat surface. There should be no bend in the leads and they should be at right angles to the body.
10. Before switching on any power supplies, hold the board up against a powerful lamp and inspect both sides with a magnifying glass for solder splashes, unsoldered joints, incorrectly orientated components and bent IC pins. (To check for the latter look at all ICs end on). TAKE TIME OVER THIS.

11. The following tools are needed:-

- (a) Long nose pliers
- (b) Side cutters
- (c) 15 to 25 watt soldering iron
- (d) A damp sponge or cloth - to keep iron bit clean
- (e) A powerful light source
- (f) A magnifying glass - for inspecting the PCB
- (g) A multimeter - not necessary, but useful to check supplies

 COMPONENT LIST

No.	Part No.	Qty	Description	Circuit ref.
INTEGRATED CIRCUITS				
01	501-244	4	74LS244 Octal Tri-state buffer	IC25 to 28
02	501-075	1	74LS75 Quad latch	IC29
03	501-156	2	74LS156 0'c 2 to 4 decoder	IC30 & 31
04	502-074	1	74S74 Schottky dual D-type flip-flop	IC32
05	503-157	2	74157 TTL Quad 2 to 1 multiplexer	IC33 & 34
06	501-020	1	74LS20 Dual 4 input Nand gate	IC35
07	501-008	2	74LS08 Quad 2 input And gate	IC36 & 41
08	501-032	2	74LS32 Quad 2 input Or gate	IC37 & 38
09	503-006	1	7406 TTL 0'c Hex inverter	IC 38 39
10	501-279	1	74LS279 Quad reset/set latch	IC40
11	501-004	1	74LS04 Hex inverter	IC46
12	601-900	1	54-018 Polara 150ns active delay line	IC47
MEMORY				
13a	024-100	8	MK4116 Dynamic RAM / 16K kit	IC1 to 8
13b	024-101	16	MK4116 Dynamic RAM / 32K kit	IC1 to 16
13c	024-102	24	MK4116 Dynamic RAM / 48K kit	IC1 to 24
RESISTORS				
14	614-100	1	✓ 899-3-R33 33R resistor pack	RP1
15	614-103	1	✓ 899-3-R47 47R resistor pack	RP2
16	614-101	1	✓ 898-1-R4.7K 4K7 resistor pack	RP 4
17	614-102	1	✓ 899-3-R4.7K 4K7 resistor pack	RP 5
18	510-272	6	2K7 .25watt red - violet - red	R1 to 6
19	510-102	4	1K .25watt brown - black - red	R7,8,9,14
20	510-221	4	220R.25watt red - red - brown	R10 to 13

RESISTORS Cont

21	510-220	1	22R .25watt red - red - black	R15
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CAPACITORS

22	609-127	1	10uF Tantalum bead 25v	C78
23	609-110	6	2uF2 Tantalum bead 35v	C74 to 76 & C80 to 82
24	520-104	48	100n Ceramic disc	C1 to 48
25	520-103	24	10n Ceramic disc	C49 to 69 71,72 & 77
26	520-330	2	33pf Ceramic disc	C70 & 79

IC SOCKETS

27	705-104	6	20 pin .3 inch DIL
28	705-102	31	16 pin .3 inch DIL
29	705-101	15	14 pin .3 inch DIL

MISCELLANEOUS

30	705-113	1	20 pin header plug .3 inch DIL	SKT 1
31	710-100	1	77 way Nasbus connector	PL 1
32	024-200	1	RAM B PCB	

SUGGESTED ORDER OF CONSTRUCTION

1. Unpack the kit and check the contents against the parts list. Return the memory ICs to their antistatic packing immediately after checking. Inspect the printed circuit board (PCB) for any signs of damage.

2. RESISTORS Preform the leads of the 15 resistors to a separation of 1/2inch (12.7mm). Some resistors may be supplied already formed. Insert the resistors into the card. Components may be held in place after insertion by bending the leads about 40 degrees in the opposite direction. Solder the resistors.

3. IC SOCKETS Check to see that all the IC sockets do not have their pins bent or missing. During insertion take care not to bend any pins. When soldering the IC sockets it may be a good idea to solder only two pins on opposite corners to begin with. Then turn the board over again and check that the sockets are flat on the board, straight and also correctly oriented. See figure 1 for typical socket orientation marks. Any necessary alterations may now be carried out with ease, as only two pins are soldered.

fig.1a Pin 1 on PCB Legend.

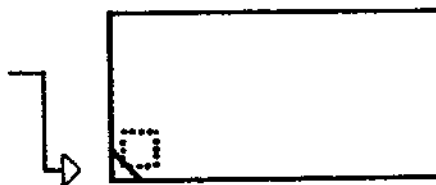
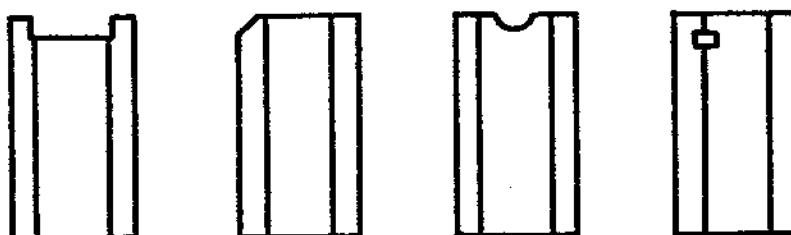
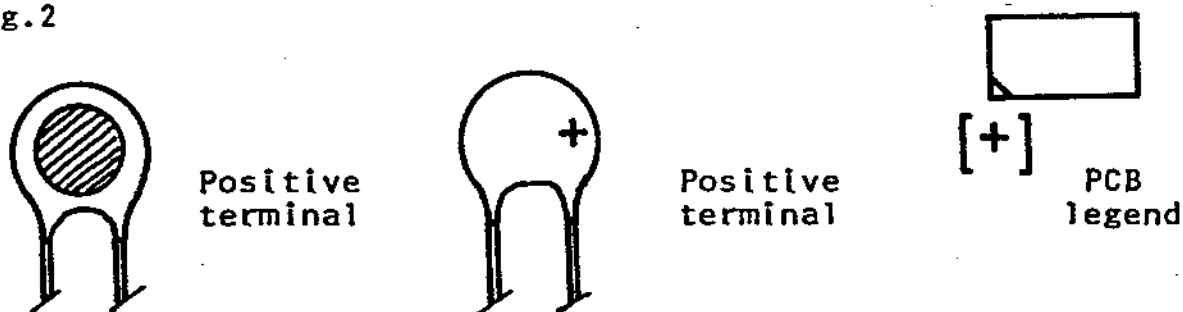


fig.1b Typical orientation marks viewed from above, pins facing away from you. Pin 1 is the top left hand corner in each case.



4. CAPACITORS Insert and solder:- (1) The 48, 100n ceramic capacitors, located near the memory array which are C1 to C48. (2) The 24, 10n ceramic capacitors. (3) The 2, 33pf ceramic capacitors which are C70 and C79. (4) And finally the tantalum capacitors. These are electrolytic capacitors and as such must be correctly orientated (see fig.2), C78 is 10uF. C74 to C76 and C80 to C82 are 2.2uF.

fig.2



5. Using offcuts from the resistors or capacitors, solder in position the test points marked with a square on the PCB. The GND (0v) test point is located near the 77 way edge connector. The remaining test points are located near the opposite edge of the PCB. These test points are, from left to right WR EN, RD EN, MUX, WR2, WR1, RAS0, CAS, RAS2, WR0 and RAS1. Crop the leads on the component side of the board leaving about 3/8ths inch or enough lead to enable test hooks to be hooked onto them. Crop the leads on the circuit side.

6. LINKS If the "Page mode and write protect upgrade kit" is not installed and memory type MK4116 is used wire the links as shown overleaf:-

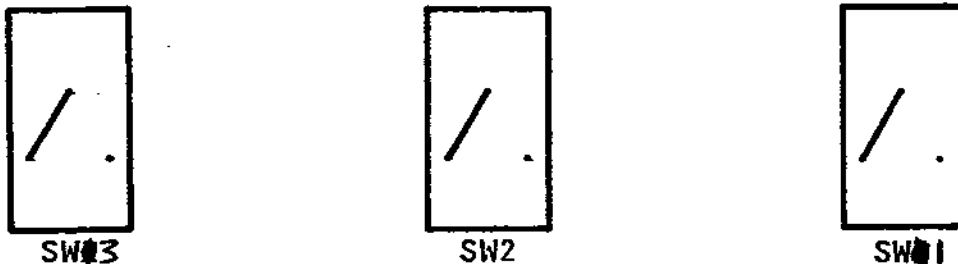
LK1 c to 2
 LK2 c to 2
 LK3 c to 2
 LK5 c to 1
 LK6 c to 2
 LK7 leave out

If the upgrade kit is installed and memory type MK4116 is used wire the links as follows:-

LK1 c to 2
 LK2 c to 2
 LK3 c to 2
 LK5 c to 2
 LK6 c to 1
 LK7 wire in link

Please note that incorrect positioning of LK1,2 and 3 may result in the memory being damaged. For further information on link options refer to section 3-4 of this manual. Finally, a link should be inserted in each of the three switch pads (SW1 to 3) when the upgrade kit is not used, as illustrated below.

fig.3 Write protect Switch Links



6. ADDRESS DECODE Insert the 20 pin header plug into SK1. One corner of the plug has a notch in it, this is pin 1. It is suggested that the address decode links are soldered onto the header while inserted into SK1. This will maintain the pin alignment while the pins are hot. Refer to section 3-5 of this manual and wire in position the decode links on the header plug.

7. INTEGRATED CIRCUITS Insert the resistor packs and ICs in the following sequence:-

- | | | |
|---------|-----------------|-----------------------------------|
| (1) | RP1..... | 899-3-R33 |
| (2) | RP2..... | 899-3-R47 |
| (3) | RP4..... | 898-3-R4.7 |
| (4) | RP5..... | 899-3-R4.7K |
| (5) | IC25 to 28..... | 74LS244 |
| (6) | IC33 & 34..... | 74157 |
| (7) | IC39..... | 7406 |
| (8) | IC46..... | 74LS04 |
| (9) | IC32..... | 74LS74 <i>OR 74S74</i> |
| (10) | IC36 & 41..... | 74LS08 |
| (11) | IC29..... | 74LS75 |
| (12) | IC35..... | 74LS20 |
| ** (13) | IC47..... | 54-018 |
| (14) | IC37 & 38..... | 74LS32 |
| (15) | IC40..... | 74LS279 |
| (16) | IC30 & 31..... | 74LS156 |
| (17) | IC1 to 8..... | MK4116 for 16K bytes
of memory |
| | IC1 to 16..... | MK4116 for 32K bytes
of memory |
| | IC1 to 24..... | MK4116 for 48k bytes
of memory |

** IC 47 (the delay line) has pin 1 indicated by a white dot.

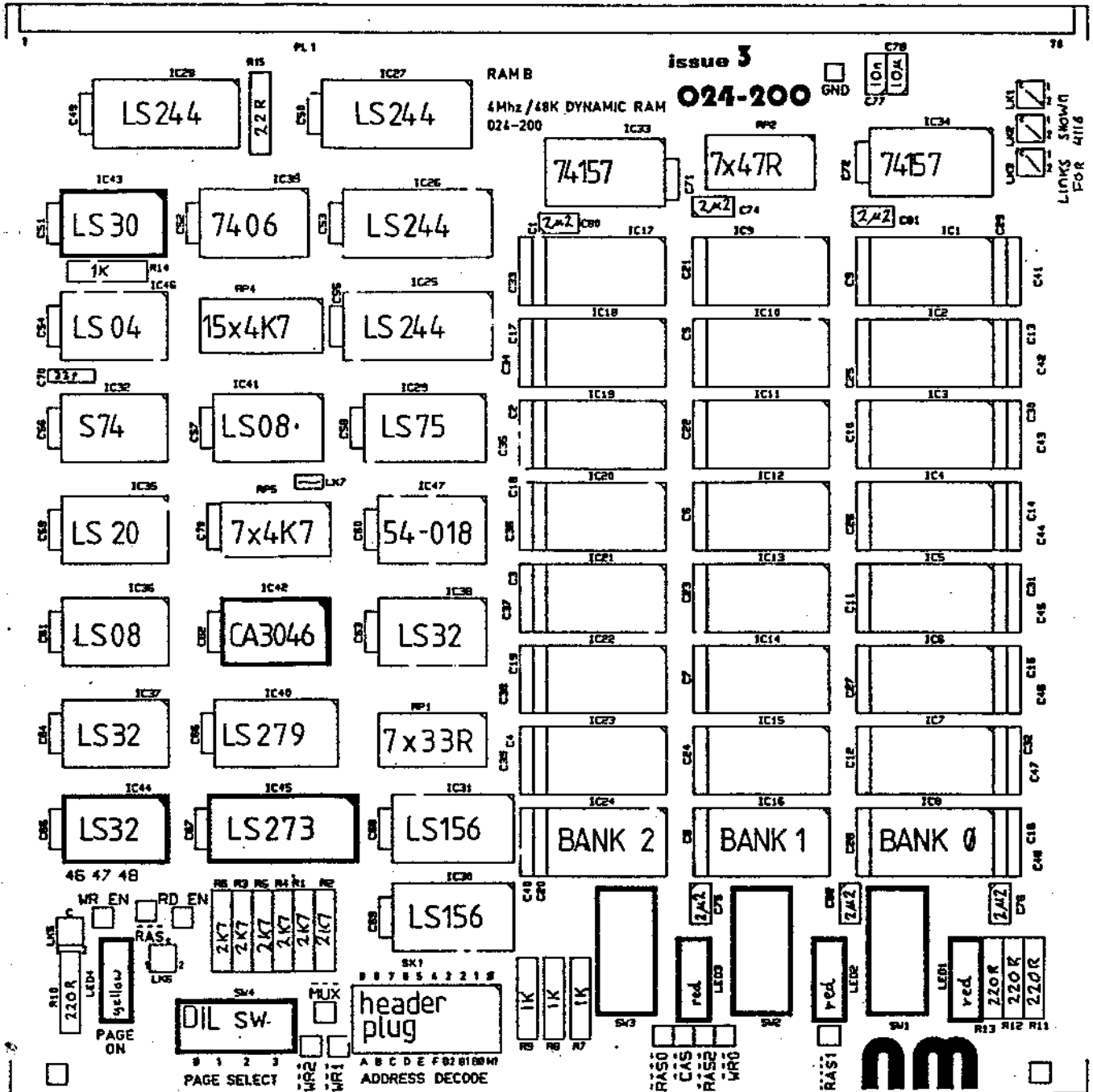
When completed, check that ICs are correctly orientated and in the right place.

8. Take a final look at the card and check that there are no unsoldered pins or solder bridges anywhere.

9. When satisfied everything is correct, plug the board into the system. Power up the system and, if a multimeter is available, check the supply voltages. Check Nascom 1 or 2 for Normal operation.

10. Enter the machine code "Memory test" program which may be found in section 2 page 1.

fig.4 Component placement RAM B 026



SECTION 2

1. MEMORY TEST PROGRAM.

This program is designed to run under Nas-sys on a Nascom 1 or 2. The program is split into two halves, part 1 executes three tests giving the following error letter if the condition is not met :-

- A - Location not set to zero
- B - Walking bit test
- C - location not set to FF

Part two of the program loads a jump instruction into each location and then executes it, moving the jump through the memory as it goes. If the program "crashes" because of a fault in memory the screen will hold the last address, or if this is cleared or corrupted locations 0D49 & 0D4A will still contain it. The program will loop till a system reset or fault occurs.

Execute 0C80 ssss eeee . Where ssss is the first location and eeee is the last location of memory to be tested.

ZEAP Z80 Assembler - Source Listing

```

                                0290 ; NAS-SYS EQUATES
0C0E                          0300 ARG2 EQU #0C0E
0C10                          0310 ARG3 EQU #0C10
0C29                          0320 CURSOR EQU #0C29
0018                          0330 SCAL EQU #18
0028                          0340 PRS EQU #28
0030                          0350 ROUT EQU #30
0066                          0360 TBCD3 EQU #66
0068                          0370 B2HEX EQU #68
0069                          0380 SPACE EQU #69
006A                          0390 CRLF EQU #6A
000C                          0400 CS EQU #0C
000D                          0410 CR EQU #0D
                                0420 ;
                                0430 ;
                                0440 ;
0C80                          0450 ORG #0C80
0C80 EF                       0460 RST PRS
0C81 0C                       0470 DEFB CS,0
0C83 EF                       0480 LOOP RST PRS
0C84 4D                       0490 DEFM /MEMORY TEST PART 1/
0C96 0D                       0500 DEFB CR,0

```

0C98	2A100C	0510		LD	HL,(ARG3);	FINISH ADDR
0C9B	AF	0520		XOR	A	
0C9C	ED5B0E0C	0530		LD	DE,(ARG2);	START ADDR
0CA0	ED52	0540		SBC	HL,DE	;CALC COUNT
0CA2	E5	0550		PUSH	HL	;COUNT ON STACK
0CA3	44	0560		LD	B,H	
0CA4	4D	0570		LD	C,L	;AND IN BC
0CA5	2A0E0C	0580		LD	HL,(ARG2)	
0CA8	E5	0590		PUSH	HL	;START ADDR ON STACK
0CA9	54	0600		LD	D,H	
0CAA	5D	0610		LD	E,L	;AND DE
0CAB	13	0620		INC	DE	;READY FOR LDIR
0CAC	3600	0630		LD	(HL),0	;ZERO THE 1st LOCATION
0CAE	EDB0	0640		LDIR		;AND COPY IT THROUGH
0CB0	E1	0650		POP	HL	;START ADDR BACK
0CB1	C1	0660		POP	BC	;AND COUNT
		0670				;CHECK FOR ZERO'S
0CB2	1600	0680	ZCHK	LD	D,0	;CLEAR ERROR FLAG
0CB4	AF	0690		XOR	A	;CLEAR A
0CB5	BE	0700		CP	(HL)	;MEMORY SHOULD BE ZERO
0CB6	3E41	0710		LD	A,"A	;LOAD ERROR LETTER IN CASE
0CB8	C4390D	0720		CALL	NZ,ERR	;FAULT A IF NON-ZERO
		0730;				-----WALKING BIT TEST
0CBB	3E01	0740		LD	A,1	;INITIAL BIT POSITION
0CBD	77	0750	WALK	LD	(HL),A	;PUT IT IN MEMORY
0CBE	BE	0760		CP	(HL)	;DID IT GET THERE
0CBF	F5	0770		PUSH	AF	;SAVE BIT PATTERN
0CC0	3E42	0780		LD	A,"B	;LOAD ERROR LETTER IN CASE
0CC2	C4390D	0790		CALL	NZ,ERR	;FAULT B IF WALK FAILS
0CC5	F1	0800		POP	AF	;BIT PATTERN AND FLAGS
0CC6	2003	0810		JR	NZ,ALFF	;IF IT FAILED DO NEXT TEST
0CC8	17	0820		RLA		;WALK BIT ACROSS
0CC9	30F2	0830		JR	NC,WALK	;UNTIL IT REACHES CARRY
		0840;				-----LOAD FF TEST
0CCB	3EFF	0850	ALFF	LD	A,#FF	
0CCD	77	0860		LD	(HL),A	
0CCE	BE	0870		CP	(HL)	;DID IT GET THERE
0CCF	3E43	0880		LD	A,"C	;LOAD ERROR LETTER IN CASE
0CD1	C4390D	0890		CALL	NZ,ERR	;FAULT C FF NOT LOADED
0CD4	7A	0900		LD	A,D	;GET ERROR FLAG
0CD5	B7	0910		OR	A	;NON-ZERO IF ERROR OCCURED
0CD6	C4460D	0920		CALL	NZ,NEWLIN	
0CD9	EDA0	0930		LDI		;STEP ON TO NEXT LOCATION
0CDB	EAB20C	0940		JP	PE,ZCHK	;LOOP TILL END REACHED

```

0950;-----PART TWO
OCDE EF      0960      RST  PRS
OCDF OD      0970      DEFB CR
OCE0 50      0980      DEFM /PART 2  OP-CODE FETCH TEST/
OCFA OD      0990      DEFB CR,0
OCFC 2A100C  1000      LD   HL,(ARG3)
OCFF AF      1010      XOR  A
OD00 ED580E0C 1020      LD   DE,(ARG2)
OD04 ED52    1030      SBC  HL,DE      ;CALC COUNT
OD06 44      1040      LD   B,H
OD07 4D      1050      LD   C,L      ;COUNT IN BC
OD08 0B      1060      DEC  BC
OD09 0B      1070      DEC  BC      ;MAKE ROOM FOR JP
OD0A EB      1080      EX  DE,HL     ;HL=ARG2
OD0B E5      1090  OPLOOP PUSH HL      ;START ADDR
OD0C 3EC3    1100      LD   A,#C3
OD0E 77      1110      LD   (HL),A
OD0F 23      1120      INC  HL      ;PUT JP IN MEMORY
OD10 11270D  1130      LD   DE,RETURN
OD13 73      1140      LD   (HL),E
OD14 23      1150      INC  HL
OD15 72      1160      LD   (HL),D   ;FOLLOWED BY ADDRESS
OD16 E1      1170      POP  HL      ;GET START ADDR BACK
OD17 ED5B290C 1180      LD  DE,(CURSOR);GET CURRENT CURSOR
OD18 C5      1190      PUSH BC     ;SAVE COUNT
OD1C DF      1200      RST  SCAL
OD1D 66      1210      DEFB TBCD3   ;PRINT CURRENT ADDR
OD1E 22490D  1220      LD  (STORE),HL ;SAVE ADDR WE MAY BOMB
OD21 ED53290C 1230      LD  (CURSOR),DE;REPLACE OLD CURSOR
OD25 C1      1240      POP  BC     ;GET COUNT BACK
OD26 E9      1250      JP   (HL)   ;JUMP TO TEST RAM
OD27 EDA0    1260  RETURN LDI      ;RETURN HERE HOPFULLY
OD29 EA0B0D  1270      JP   PE,OPLOOP;LOOP TILL DONE
OD2C EF      1280      RST  PRS
OD2D 4C      1290      DEFM /LOOPING/
OD34 0D      1300      DEFB CR,0
OD36 C3830C  1310      JP   LOOP
1320;-----ERROR ROUTINE
OD39 F5      1330  ERR  PUSH AF     ;SAVE FLAGS
OD3A F7      1340      RST  ROUT   ;OUTPUT ERROR LETTER
OD3B DF      1350      RST  SCAL
OD3C 69      1360      DEFB SPACE  ;AND SPACE
OD3D C5      1370      PUSH BC    ;SAVE COUNT
OD3E DF      1380      RST  SCAL
OD3F 66      1390      DEFB TBCD3  ;OUPUT ADDR
OD40 C1      1400      POP  BC
OD41 DF      1410      RST  SCAL
OD42 69      1420      DEFB SPACE
OD43 14      1430      INC  D      ;SET ERROR FLAG

```

0D44 F1	1440	POP	AF	
0D45 C9	1450	RET		
0D46 DF	1460	NEWLIN	RST	SCAL
0D47 6A	1470	DEFB	CRLF	
0D48 C9	1480	RET		
0002	1490	STORE	DEFS 2	;SPACE FOR ADDR

Memory test object code listing

```

0C80 EF 0C 00 EF 4D 45 4D 4F 52 59 20 54 45 53 54 20
0C90 50 41 52 54 20 31 0D 00 2A 10 0C AF ED 5B 0E 0C
OCA0 ED 52 E5 44 4D 2A 0E 0C E5 54 5D 13 36 00 ED B0
OCB0 E1 C1 16 00 AF BE 3E 41 C4 39 0D 3E 01 77 BE F5
OCC0 3E 42 C4 39 0D F1 20 03 17 30 F2 3E FF 77 BE 3E
OCD0 43 C4 39 0D 7A B7 C4 46 0D ED A0 EA B2 0C EF 0D
OCE0 50 41 52 54 20 32 20 20 4F 50 2D 43 4F 44 45 20
OCF0 46 45 54 43 48 20 54 45 53 54 0D 00 2A 10 0C AF
0D00 ED 5B 0E 0C ED 52 44 4D 0B 0B EB E5 3E 77 23
0D10 11 27 0D 73 23 72 E1 ED 5B 29 0C C5 DF 66 22 49
0D20 0D ED 53 29 0C C1 E9 ED A0 EA 0B 0D EF 4C 4F 4F
0D30 50 49 4E 47 0D 00 C3 83 0C F5 F7 DF 69 C5 DF 66
0D40 C1 DF 69 14 F1 C9 DF 6A C9 00 00 00 00 00 00

```

Upon execution of the above program the VDU should output the following message if the Memory card is functions correctly.

MEMORY TEST PART 1

PART TWO OPCODE FETCH TEST
LOOPING

This message will be repeated until either a fault condition arrises or a system reset is performed.

However if the Memory card is faulty the VDU would output a message similar to the example below;-

MEMORY TEST PART 1

```

A aaaa B bbbb C cccc
A aaaa B bbbb C cccc
A aaaa
A aaaa
A aaaa B bbbb
A aaaa B bbbb C cccc

```

PART 2 OPCODE FETCH TEST
eeee

Where aaaa is a location in memory that will not set to zero, bbbb will not accept certain data patterns, cccc will not set all bits high & eeee was the last address that did not accept a jump command.

Memory test program copyright c 1980 CC Soft.

SECTION 3

1. SPECIFICATIONS

Memory capacity.....	max. 48K bytes in 16K increments
Memory cycle time (without wait state).....	400ns min.
Memory access time (without wait state).....	150ns max.
Operating temperature.....	0C to 50C
Interface levels.....	TTL compatible
Supply requirements.....	+12v +/- 5% @ 130mA typ. (fully populated)
	+5v +/- 5% @ 300mA typ.
	-5v +/- 5% @ 25mA typ.
Physical dimensions.....	8 x 8 inches
Bus structure.....	to Nasbus Issue 4 specification

2. NASBUS MEMORY ASSOCIATED CONTROL SIGNALS

$\overline{\text{MREQ}}$	Memory request indicates that the address bus holds a valid address for memory read, write or refresh.
$\overline{\text{RFSH}}$	Refresh indicates that the lower seven bits of the address bus contain a refresh address for dynamic memory.
$\overline{\text{RD}}$	Read indicates that the CPU wants data from I/O or memory.
$\overline{\text{WR}}$	Write indicates that the data bus holds valid data for memory to store
$\overline{\text{RAMDIS}}$	RAM disable is an active low signal which disables output from any RAM on the bus. Used to give ROM priority over RAM.
$\overline{\text{M.EXT}}$	A decoded signal from one of the RAM boards in the system defining which 4K block is used by Nascom 1. Not used by Nascom 2.

DBDR Data bus drive determines the direction of the bidirectional data bus buffers on the buffer card. Low to drive data to the Nascom. Not used by Nascom 2.

The following circuit description should be read in conjunction with the circuit diagrams to be found near the end of this manual.

3. ADDRESS and DECODE LOGIC Address lines A0 to A11 are buffered by ICs 27 and 28 (Schottky Schmitt). Buffered address lines A0 to A13 are routed to address switches IC33 and 34, where they are switched into the memory array to provide row (A0 to A6) and column (A7 to A13) addresses. The row and column addresses are strobed into the memory by two negative going clocks called Row address strobe (RAS) and column address strobe (CAS). By the use of RAS and CAS the address bits are latched into the memory for access to the required memory location. Because the Z80 CPU does not guarantee that the address bus will hold valid information past the rising edge of MREQ on an Op-code fetch, A12 to A15 are latched (IC29) each time MREQ is active. This prevents glitches appearing on the RAS lines. A12 to A15 are decoded in ICs 30 and 31 to provide select signals for each 4K byte block of memory starting at any 4K boundary. These signals arrive at pins 1 to 16 of SK1. Pin 20 of SK1 provides the M.EXT signal which is necessary to decode the internal addressing of Nascom 1. This signal is not required by Nascom 2. Pins 17, 18 and 19 (SK1) are the memory array bank selects. These selects should be commoned to four of the 16 4K decodes. A0 to A7 are also routed to IC43 for Port decoding when "Page-mode" is used.

4. MEMORY CONTROL LOGIC MREQ is buffered by IC 27/3 and inverted by IC46/8. The output from IC46/8 is Anded (IC36/11) with the output from the 4Mhz Z80 precharge extender circuit (IC32) and is then inverted by IC46/10 (TP9-RAS). The RAS signal is then Ored in IC37/3/6/8 with the Anded bank decode and Refresh signals. When a memory bank is decoded only one RAS line to the memory array goes low. However, if a memory refresh is being performed, all the RAS inputs to the array will go low. The Active delay line (IC47), whose input is MREQ, goes low at pin 4 (MUX) approximately 60ns after MREQ goes active. All memory timing is referenced to MREQ. The 60ns delay was chosen to allow an adequate margin for the row address hold time. The signal controls the address multipliers (IC33 & 34). Until now the memory array has been receiving the row addresses (A0 to A6). When MUX goes low the

column addresses (A7 to A13) are then switched to the array address inputs. After a further delay of approximately 30ns the delay line goes low at Pin 11 (CAS). This signal is then Ored in IC37/11 with RFSH. If a refresh is not being performed the memory array will receive CAS. It is necessary to delay CAS from MUX in order to allow the addresses to stabilise after being switched. When CAS is received the memory then latches the column addresses.

5. READ and WRITE LOGIC The \overline{WR} signal is buffered in IC27/7 and is then Ored with the output of the card page mode WREN circuitry (TP10). This line is taken to the common terminal of LK5. If page mode is not installed then LK5/C should be connected to LK5/1 (+5v). This will permanently enable write enable. However, if page mode is installed, this link should be connected the other way round (LK5/C to LK5/2). This connects the WREN signal to the page mode circuitry and only when the card is paged in, will WREN be enabled. This signal is active high. The combined \overline{WR} and WREN signal is then further Ored within the remaining three gates of IC38 with the memory bank write protect signals from IC40/4, 7 & 9. The outputs of IC38 are taken to the memory array \overline{WR} inputs via 3 33R resistors within RP1. The \overline{WR} inputs to the memory array also appear at TP6, 7 & 8 where they are marked WR 0 - 2 on the PCB. The write protect switches are supplied with the page mode kit (SW 1 - 3) so when the card is not used in page mode it is necessary to install 3 links, one in each of the switch pads; as shown in Fig.3 Because these write protect inputs are fully buffered, it is possible to have SW 1 - 3 mounted in a remote site not too far away from the card and connected to the 3 pads of each switch. The RD input is buffered in IC39/4 which appears at an input of IC35/8. The other inputs to this gate are MREQ, decode and card RDEN. The output of the gate when active enables the data output buffer IC25 and will bring Nasbus \overline{DBDR} low. The memory will output data when addressed only when its write inputs are not active. (For further information on the memory chips, refer to Mostek's data sheet on the MK4116). The card RDEN (TP11) signal is similar to the previously mentioned WREN signal. When page mode is not installed, it is necessary to link LK6/C to LK6/2. LK6/C should be linked to LK6/1 if page mode is installed.

6. PAGE MODE and write protect upgrade kit. IC43 decodes the port (port FF) and is Ored with \overline{WR} in IC44/3. This signal is subsequently Ored with \overline{TORQ} which is used as a clock to latch data into IC45. The outputs from IC45 will all be low on power-up as the system reset is connected to the master reset input of this IC. Also on power-up, IC40/13 will be high bringing IC44/8 & 11 high. SW4 is a four position d11 switch which selects the card page number. If in position 0 as marked

on the PCB, the card will become active on power-up and up until such time as the port status changes. By changing the data of port FF one card can be paged out and another paged into the system. Because of this method of paging it is possible to enable one card to read only and another to write only; so by allowing the processor to read and write to the same address, data will be transferred from one page to another. This illustrates only one of many ways in which the page mode facility can be used. The page on LED (LED4) will be lit up when a page is read enabled. LED1, 2 & 3 will be lit if the write protect switch is in its protect position. These LEDs are driven by IC42 which is a five NPN transistor array. The fifth transistor in this package is used to provide Nasbus with an $\overline{IO/EXT}$ signal. When page mode is not installed, LK7 should not be present. Nasbus lines 46 to 48 are brought onto the card to allow the facilities of the page mode to be extended at a later date.

7. SUGGESTED NASCOM MEMORY MAP

2k	0000 to 07FF	Existing operating system
1k	0800 to 0BFF	Existing video RAM
128	0C00 to 0C7F	Existing operating system workspace
80	0C80 to 0CFF	Extended operating system workspace
	0D00 to 0F7F	Workspace for firmware or workspace for programs
	0F80 to 0FFF	Usual stack space
	1000 to 8FFF	General RAM space. Start of general program space
	9000 to 9FFF	Programmable graphics RAM or general RAM space
	9800 to AFFF	Colour graphics RAM or general RAM space
	B000 to B7FF	Extensions to the operating system or extensions to Naspen
	B800 to BFFF	Naspen or related word processing software
	C000 to CFFF	Revas or general disassembler software or Colour graphics control software

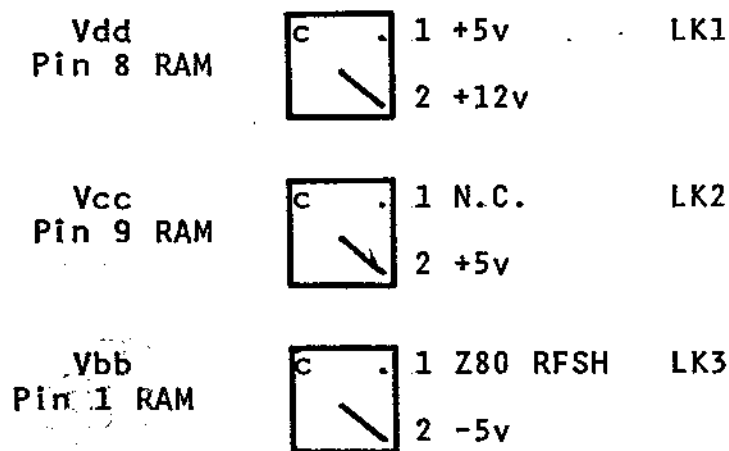
Memory map continued...

D000 to DFFF or general assembler type software or extensions to Basic

E000 to FFFF 8K Basic

8. MEMORY ARRAY SUPPLY LINKS (LK1 to 3) These three links are provided to enable memories other than type MK4116 to be used on the board. This includes new memories not yet available such as Pseudo-Static devices. If this type of device is used in the future, some makes may require the Z80 refresh signal at pin 1. In this case change LK 3 (c to 1) and remove tantalum capacitors C80, 81 and 82. Check the supply requirements for these devices and change LK1 and 2 where appropriate

fig.5 Links 1 to 3



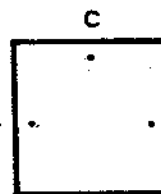
The above links 1 to 3 are shown in the correct position for use with MK4116 Dynamic memory, as supplied with the kit.

9. PAGE MODE LINKS (LK5 to 6)

fig.6

WR.EN
LK5

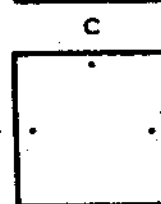
Page mode not
installed 1



2 Page mode
installed

RD.EN
LK6

Page mode
installed 1



2 Page mode not
installed

I/O EXT
LK7

Page mode
installed



Page mode not
installed
(no link)

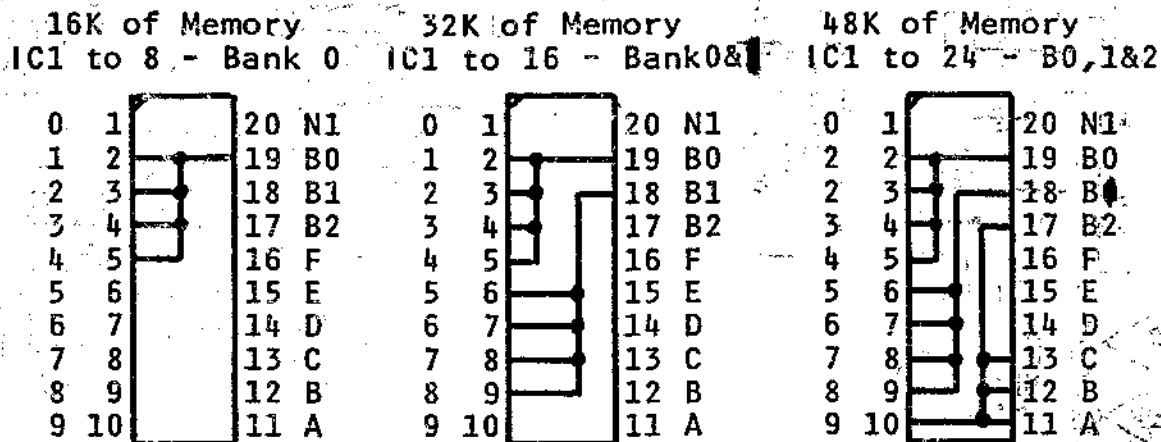
10. ADDRESSING LINK OPTIONS

fig.7 SK1 Address decode

0000-0FFF	1	20	N1 M.EXT
1000-1FFF	2	19	BANK 0 (ICs 1 to 8)
2000-2FFF	3	18	BANK 1 (ICs 9 to 16)
3000-3FFF	4	17	BANK 2 (ICs 17 to 24)
4000-4FFF	5	16	F000-FFFF
5000-5FFF	6	15	E000-EFFF
6000-6FFF	7	14	D000-DFFF
7000-7FFF	8	13	C000-CFFF
8000-8FFF	9	12	B000-BFFF
9000-9FFF	10	11	A000-AFFF

A link between pin 1 and 20 is only requisite if the memory card is to be used in a Nascom 1 system.

fig.8 Suggested link options.



11. References

1. Z80 CPU Technical manual
2. Nasbus functional specification. Issue 7.
3. MOSTEK MK4116 RAM data sheet
4. Nascom 1 constructional notes
5. Nascom 2 constructional notes
6. Nascom Buffer card specification.
7. MOSTEK Z80 Dynamic RAM interface application note.

This documentation was prepared on the NAS-PEN Text processor.