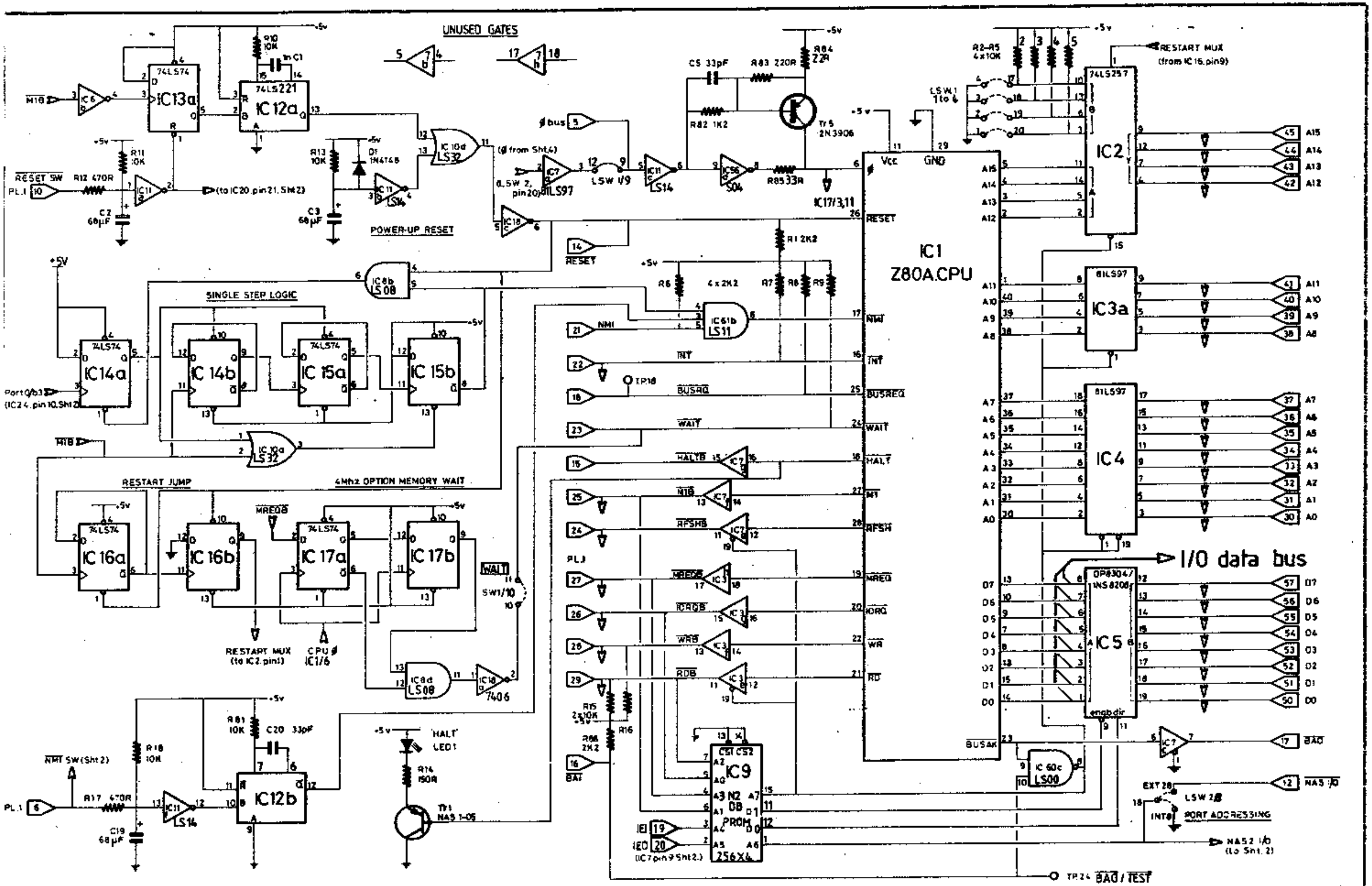
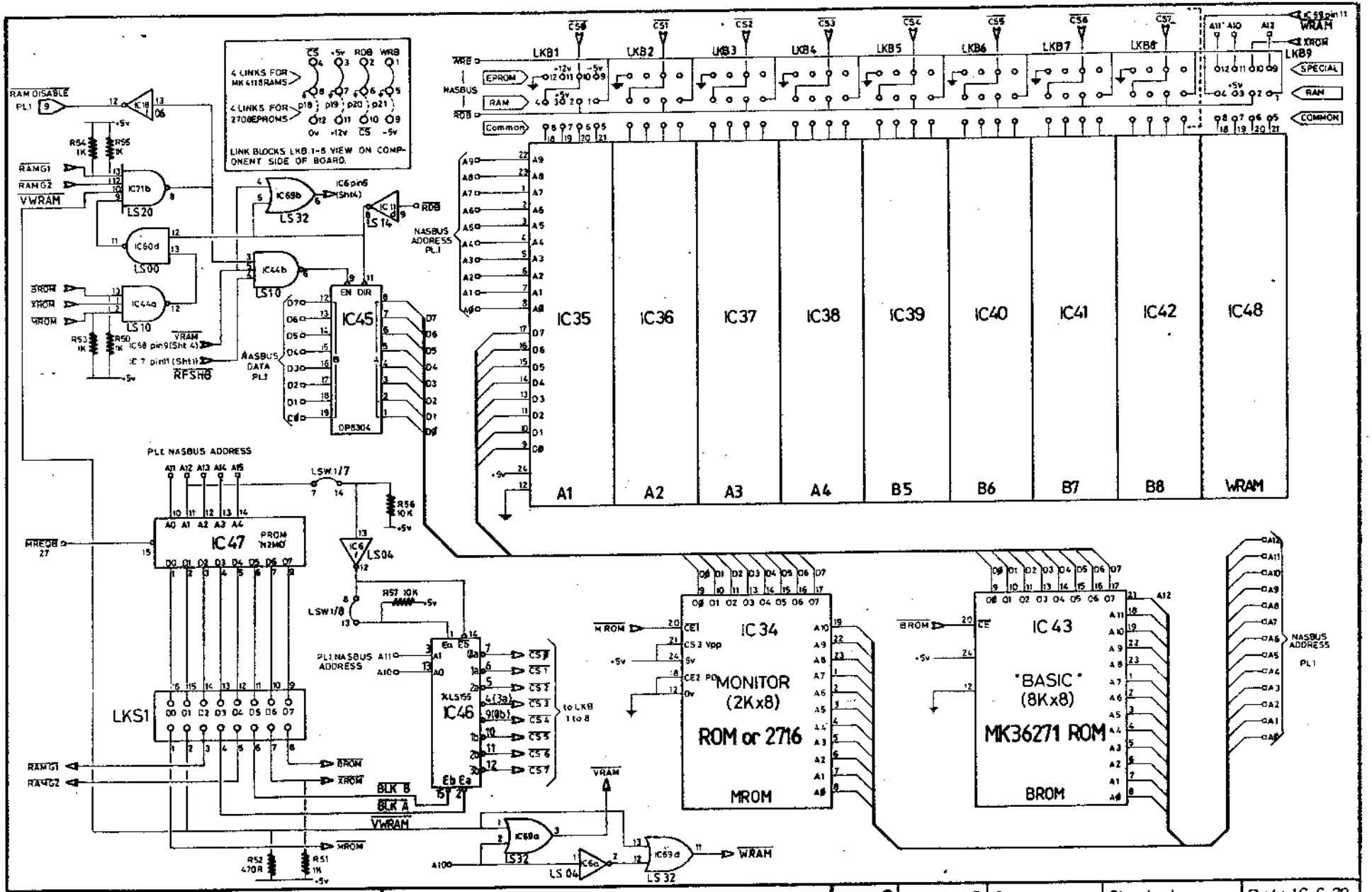
7-1 Circuit Diagrams


UNUSED GATES
SINGLE STEP LOGIC
RESTART JUMP
4MHz OPTION MEMORY WAIT
POWER-UP RESET
IC1
Z80A.CPU
IC2
74LS257
IC3a
81LS97
IC4
81LS97
IC5
DP8304/
INS8208
IC9
N2
DB
PROM
256X4
IC12a
74LS221
IC12b
IC13a
IC14a
IC14b
IC15a
IC15b
IC16a
IC16b
IC17a
IC17b
74LS74
I/O data bus
RESTART MUX
(from IC16,pin9)
RESTART MUX
(to IC2,pin1)
CPU ϕ
IC1/6
ϕ bus
(ϕ from Sht.4)
(to IC20,pin21,Sht2)
Port0/b3
(IC24,pin10,Sht2)
RESET SW
NMI SW(Sht2)
NAS2 I/O
(to Sht. 2)
PORT ADDRESSING
LSW 1/9
LSW1
1 to 4
LSW 2/8
SW1/10
R2-R5
4x10K
4 x 2K2
Tr5
2N3906
Tr1
NAS 1-05
'HALT'
LED1
TP18
TP24 BAO/TEST
IC17/3,11
EXT
INT
IEI
IEO
(IC7 pin 9 Sht2.)
PL.1

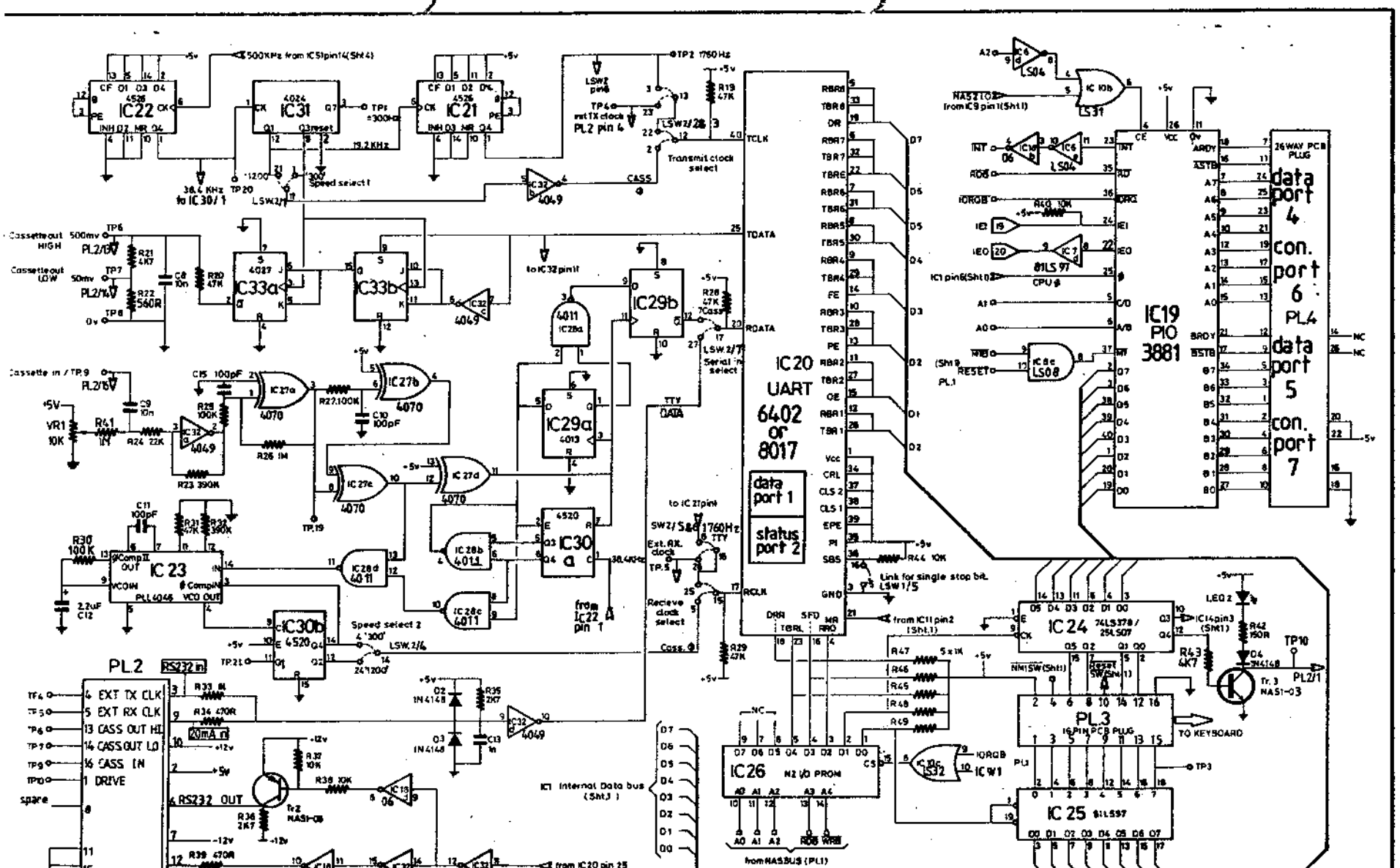
Nascom Microcomputers

NASCOM 2 CPU

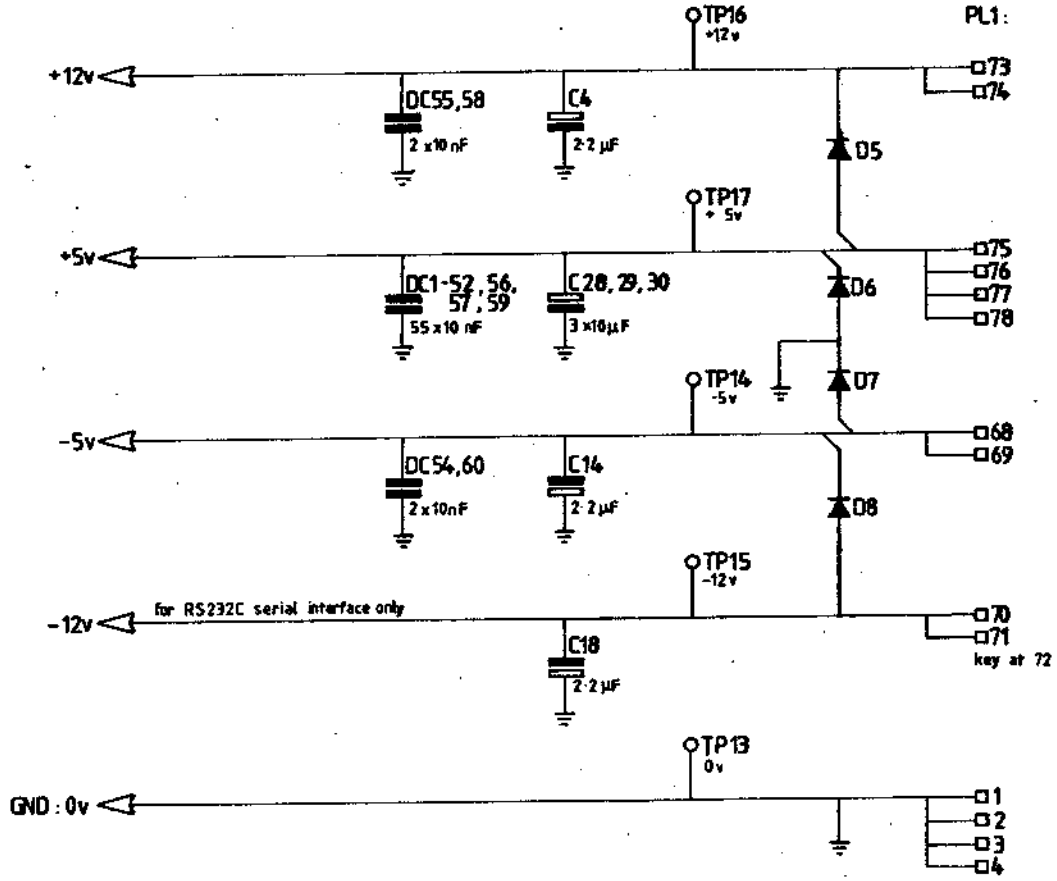
Issue 8	Sht 1 of 5	Drawn	Checked	Date 16-6-79
Revisions:- revision 6/11/10.79		Drawing no. 022-401		



Nascom Microcomputers	NASCOM 2 Memory	Issue 8	Sht 3 of 5	Drawn	Checked	Date 16-6-79
		Revisions			Drawing no. 022-403	

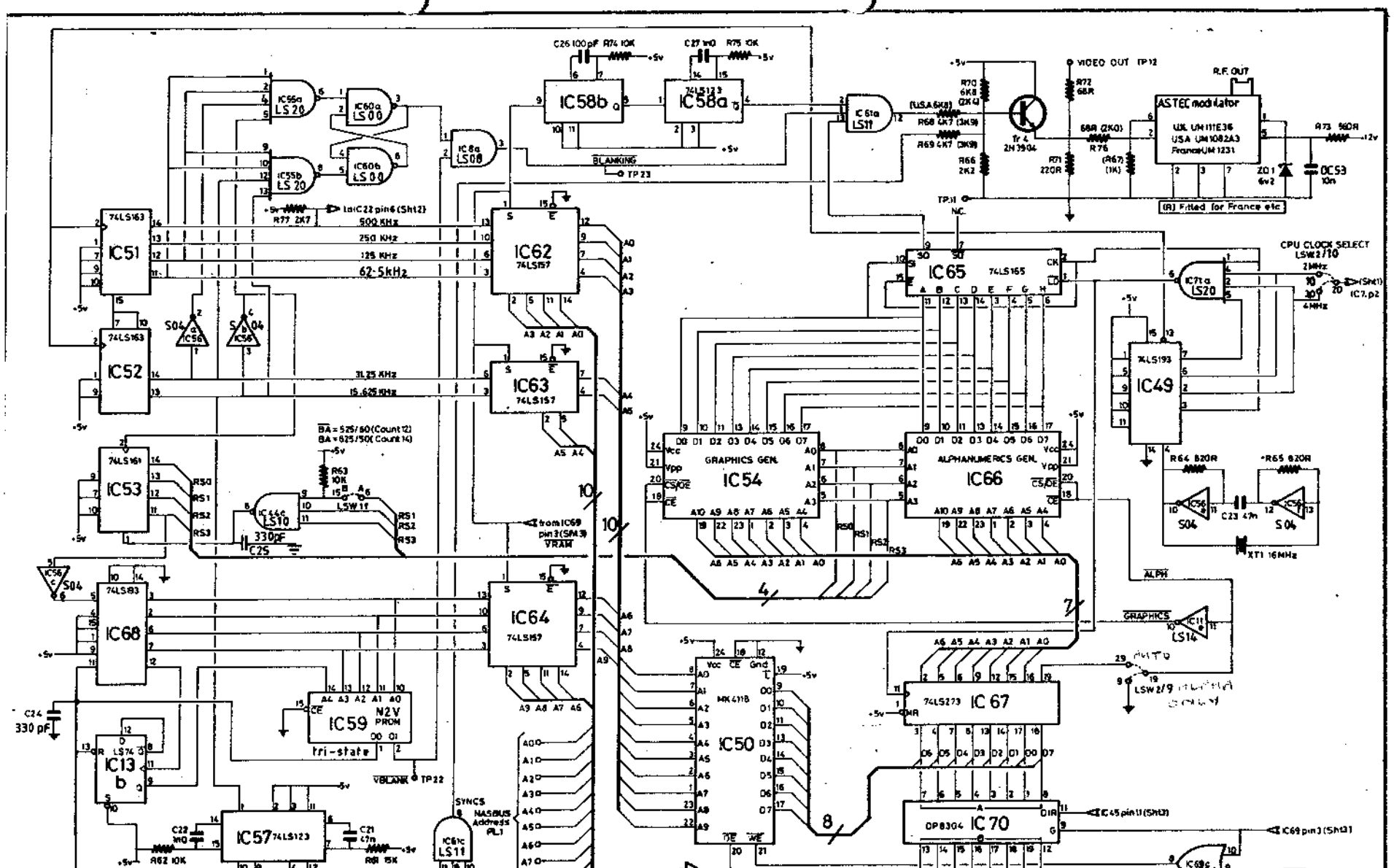


Nascom Microcomputers	NASCOM 2 — Input/Output	Issue 8	Sht 2 of 5	Drawn	Checked	Date 17-6-79
		Revisions			Drawing no	022-402



D5-7: 4 x 1N4001

Nascom Microcomputers	NASCOM 2-Power Distribution	Issue 8	Sht 5 of 5	Drawn	Checked	Date 11·10·79
		Revisions:			Drawing no. 022 - 405



Nascom Microcomputers	NASCOM 2-Video	Issue 8	Sht 4 of 5	Drawn	Checked	Date 20-6-79
		Revisions			Drawing no. 022-404

7.3 Relationship between N2MD PROM and link pins

It can be seen from circuit diagrams 3 and 4, that all on board memory (ICs 35;42, 48 and 50) is connected to address lines AØ to A9 which corresponds to ØØØØ - Ø3FFH or 1R of addresses. Additionally the MONITOR ROM is connected to AØ to A1Ø and the BASIC ROM to AØ to A12. The memory devices are enabled one at a time by means of a chip select or chip enable input, CS/CE (active low) which permits memory to be addressed at locations other than ØØØØH - Ø7FFH. The chip select function is performed by the N2MD PROM (IC47) in conjunction with the 16pin header plug (LKS1), IC6, IC46,IC69 and switches LSW1/7 and 8.

The MD PROM has 5 inputs (plus active low chip select) which are decoded by internal program, into 32 eight bit patterns, one for each combination of the input. The eight output lines are connected to one side of the 16 pin header. The outputs available from the N2MD PROM are as follows:-

	N2MD PROM INPUT						OUT-PUT BIT PATTERN								
	A15	A14	A13	A12	A11	(XXXXX DECODE)	D7	D6	D5	D4	D3	D2	D1	DØ	NORMAL USE
ØØØØH - Ø7FFH	Ø	Ø	Ø	Ø	Ø	(Ø Low Half)	1	1	1	1	1	1	1	Ø	$\overline{\text{MROM}}$ (2K MONITOR ROM)
Ø8ØØH - ØFFFH	Ø	Ø	Ø	Ø	1		1	1	1	1	1	1	Ø	1	$\overline{\text{WRAM}}$ (2K WORKSPACE RAM)
						(Ø High Half)									
1ØØØH - 1FFFH	Ø	Ø	Ø	1	Ø	(1)	1	1	1	1	1	Ø	1	1	4K USER RAM (BLKA + RAMG1)
	Ø	Ø	Ø	1	1		1	1	1	1	1	Ø	1	1	
2ØØØH - 2FFFH	Ø	Ø	1	Ø	Ø	(2)	1	1	1	1	Ø	1	1	1	4K USER RAM (BLKB + RAM G2)
	Ø	Ø	1	Ø	1		1	1	1	1	Ø	1	1	1	
	Ø	Ø	1	1	Ø	(3)	1	1	1	1	1	1	1	1	
	Ø	Ø	1	1	1		1	1	1	1	1	1	1	1	
	Ø	1	Ø	Ø	Ø	(4)	1	1	1	1	1	1	1	1	
	Ø	1	Ø	Ø	1		1	1	1	1	1	1	1	1	
	Ø	1	Ø	1	Ø	(5)	1	1	1	1	1	1	1	1	
	Ø	1	Ø	1	1		1	1	1	1	1	1	1	1	
	Ø	1	1	Ø	Ø	(6)	1	1	1	1	1	1	1	1	
	Ø	1	1	Ø	1		1	1	1	1	1	1	1	1	
	Ø	1	1	1	Ø	(7)	1	1	1	1	1	1	1	1	
	Ø	1	1	1	1		1	1	1	1	1	1	1	1	
	1	Ø	Ø	Ø	Ø	(8)	1	1	1	1	1	1	1	1	
	1	Ø	Ø	Ø	1		1	1	1	1	1	1	1	1	
	1	Ø	Ø	1	Ø	(9)	1	1	1	1	1	1	1	1	
	1	Ø	Ø	1	1		1	1	1	1	1	1	1	1	
	1	Ø	1	Ø	Ø	(A)	1	1	1	1	1	1	1	1	
	1	Ø	1	Ø	1		1	1	1	1	1	1	1	1	
BØØØH - BFFFH	1	Ø	1	1	Ø	(B)	1	1	1	Ø	1	1	1	1	4K SPARE FOR EPROM
	1	Ø	1	1	1		1	1	1	Ø	1	1	1	1	
CØØØH - CFFFH	1	1	Ø	Ø	Ø	(C)	1	1	Ø	1	1	1	1	1	4K SPARE FOR EPROM
	1	1	Ø	Ø	1		1	1	Ø	1	1	1	1	1	
DØØØH - DFFFH	1	1	Ø	1	Ø	(D)	1	Ø	1	1	1	1	1	1	4K SPARE FOR EPROM
	1	1	Ø	1	1		1	Ø	1	1	1	1	1	1	
EØØØH - FFFFH	1	1	1	Ø	Ø	(E)	Ø	1	1	1	1	1	1	1	$\overline{\text{BROM}}$
	1	1	1	Ø	1	(F)	Ø	1	1	1	1	1	1	1	8K BASIC ROM
	1	1	1	1	Ø		Ø	1	1	1	1	1	1	1	
	1	1	1	1	1		Ø	1	1	1	1	1	1	1	
						PIN NAS ON LKS 1:	9	10	11	12	13	14	15	16	

7.2 Contents of decode ROM's

I/O

```
$A0000,
FF FF FF FF FF FF FF FF FD EF DF 7F FF FF FF FF
FE FB F7 BF FF EF FF DF FF FF FF EF FF FF 7F FF
$S1EE1,
```

N2 I O/1
tristate or open collector

V

```
$A0000,
FD FC FF FF FF FF FF FF FF EF FF FD FD FD FD FF
FF FF FF FF FF FF FF FF FF EF FF FF FF FF FF FD
$S1FD1,
```

N2V/2H
tristate

---

or:

```
$A0000,
01 00 03 03 03 03 03 03 03 03 03 01 01 01 01 03
03 03 03 03 03 03 03 03 03 03 03 03 03 03 03 01
$S0051,
```

N2V/2L
tristate

MD

```
$A0000,
FE FD FB FB F7 F7 FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF EF EF DF DF BF BF 7F 7F 7F 7F
$S1CE5,
```

N2MD/3
open collector
(binary listing in text)

DB

```
$A0000,
F C F C F E F D F E D F C E D D
F C F C F E F D F E D F D E D D
F C F C F E F D F E D F C E D D
F C F C F E F D F E D F C E D D
F C F C F E F D F E C F C E D D
F C F C F E F D F E C F D E D D
F C F C F E F D F E C F C E D D
F C F C F E F D F E C F C E D D

$A0080,
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E 9 E 9 E C C
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E C E C E E E
E C E C E E E E E E C E 9 E E E
E C E C E E E E E E C E C E E E
E C E C E E E E E E C E C E E E
$S007C,
```

N2DB/3H
tristate
('H' version leaves unused output bits high)

---

or:

```
$A0000,
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 5 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 5 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5

$A0080,
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 1 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 1 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
$S057C,
```

N2DB/3L
tristate
('L' version leaves unused output bits low)

7.4 Extracts from the Mostek Z80 central processing unit tecnical manual.

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