Nascom Microcomputers

NASBUS FUNCTIONAL SPECIFICATION

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APPROVAL: A R Rundle

TITLE: NASBUS Functional Specification

CONTENTS

1. Introduction

The NASBUS is a bus used to add extra boards (e.g. memory and I/O) to the basic NASCOM Microcomputer. It consists mainly of buffered Z80 input and output signals together with some additional bus control lines.

The equipment practice used has been chosen for its wide availability and low cost.

This document defines the electrical and physical charateristics of the NASBUS.

2. References

This specification should be read in conjunction with the following documents:

1. Z80 Microcomputer devices Technical Manual
   MK 3880 Central Processing Unit - Mostek.

2. VERO catalogue.

3. Functional Description

The Nasbus is a 77 way bus, with signals allocated as described below. Please see the Z80 cpu manual (1) for details of timing and operation of Z80 derived signals.

Note that lines marked "Reserved" have already been allocated for future use. Lines marked spare may be used for any purpose but we do not guarantee not to redefine and use them in the future.

PIN	SIGNAL NAME	Description
1	Ov	Power supply and system ground
2	Ov	
3	Ov	
4	Ov	
5	Clock	2 MHZ buffered system clock
6	(spare)	
7	(spare)	
8	(spare)	
9	$\overline{\text{RAM DISABLE}}$*	An active low signal which disables output from any RAM card on the bus. Used to give ROM priority over RAM.
10	$\overline{\text{RESET SWITCH}}$ *	An active low signal which initiates a short pulse on the RESET line (pin 14), to reset the system without destroying dynamic RAM contents.
11	$\overline{\text{NASCOM MEM}}$	A decoded signal from one of the RAM boards in the system defining which 4K memory block is used by the NASCOM. (Usually 0000H - 0FFFH).
12	$\overline{\text{NASCOM 10}}$	A decoded signal from an IO extension card defining which ports are used on the NASCOM.
13	$\overline{\text{DBDR}}$ *	This signal 'Data bus drive' determines the direction of the bidirectional data bus buffers on the NASCOM Buffer card. It is a decoded signal made active by any device transferring data to the NASCOM card. Active low to drive data to the NASCOM.

PIN	SIGNAL NAME	Description
14	$\overline{\text{RESET}}$	The main system reset line. The duration of the RESET pulse is restricted to maintain dynamic RAM refresh.
15	$\overline{\text{HALT}}$	Buffered Z80 $\overline{\text{HALT}}$ signal.
16 17	$\overline{\text{BAI}}$ $\overline{\text{BAO}}$	These signals are used to provide a 'daisy chain' Bus acknowledge signal for priority bus control.
18	$\overline{\text{BUSRQ}}$ *	Z80 BUSRQ signal. Used by external devices to request control of the data, address and control lines.
19 20	IEI IEO	These signals form a 'daisy chain' connection for interrupt priority control.
21	(reserved for $\overline{\text{NMI}}$) *	On the NASCOM the Z80 Non Maskable Interrupt is dedicated to the monitor single step feature. This line is reserved for $\overline{\text{NMI}}$ for users who require this signal on the bus.
22	$\overline{\text{INT}}$ *	Z80 Interrupt request line.
23	$\overline{\text{WAIT}}$ *	Z80 $\overline{\text{WAIT}}$ line
24	$\overline{\text{RFSH}}$	Tristate buffered Z80 $\overline{\text{RFSH}}$ signal
25	$\overline{\text{MI}}$	Buffered Z80 $\overline{\text{MI}}$ signal.
26	$\overline{\text{IORQ}}$	Tristate buffered Z80 $\overline{\text{IORQ}}$
27	$\overline{\text{MREQ}}$	Tristate buffered Z80 $\overline{\text{MREQ}}$
28	$\overline{\text{WR}}$	Tristate buffered Z80 $\overline{\text{WR}}$
29	$\overline{\text{RD}}$	Tristate buffered Z80 $\overline{\text{RD}}$
30	A0	
31	A1	
32	A2	
33	A3	
34	A4	
35	A5	
36	A6	
37	A7	Tristate Z80 Address lines
38	A8	0 to 15
39	A9	

PIN	SIGNAL NAME	DESCRIPTION
40	A10	
41	A11	
42	A12	
43	A13	
44	A14	
45	A15	
46	)	
47	)	
48	) Reserved	
49	)	
50	DO	
51	D1	
52	D2	
53	D3	Bidirectional, Tristate Z80
54	D4	Data lines 0 to 7.
55	D5	
56	D6	
57	D7	
58	)	
59	)	
60	)	
61	) Reserved	
62	)	
63	)	
64	)	
65	)	
66	Unused to provide separation of signal and power lines.	
67		
68	-5V	Power supply
69	-5V	Power supply
70	-12V	" "
71	-12V	" "
72	Keyway	
73	+12V	Power Supply
74	+12V	" "
75	+ 5V	" "
76	+ 5V	" "
77	+ 5V	" "
78	+ 5V	" "

* = "Open Collector" signal line

4. Electrical Specification

4.1 Tristate Logic

These lines are driven by low power Schottky tristate buffers capable of sinking 16 mA i.e. capable of driving 10 standard TTL loads (1.6mA sinking, 40 μA source) or approximately 40 low power Schottky inputs (0.36 mA sinking, 20 μA source) while retaining logic<zero 0.4v and logic 1>2.4v.

4.2 Open Collector

Open collector lines are pulled up to 5 v. Any board can pull down to zero provided it is capable of sinking 16 mA.

4.3 Power supplies

In order to avoid overloading the motherboard and the system power supplies the following rules should be applied.

(a) All bus lines of the same voltage should be commoned on the board.

(b) No board should draw a total of more than:

+	5v	2.0 Amps
-	5v	0.5 Amp
+	12v	1.0 Amp
-	12v	0.5 Amp

(c) The whole occupied Nasbus should not draw more than:

+	5v	8 Amps
-	5v	1 Amp
+	12v	2 Amps
-	12v	1 Amp

4.4 General Design Points

Boards should be designed where possible to apply no more than 2 or 3 low power loads to any signal line of the Nasbus. In any event, a maximum of 1 TTL load must not be exceeded.

Note that tristate lines will float if the Nascom cpu is disabled e.g. by a bus request.

5. Physical Specification

5.1. Board Specification

5.1.1 Board Dimensions

The standard board size is 203.20 mm long + 0.00, - 0.30 by 203.20 mm. high + 0.00, - 0.25 (i.e. 8 x 8 inches). The thickness should be 1.60 nominal (including copper) See also Appendix A.

A suitable prototyping board is Vero type 10-0155 F (up to 45 DIPs) Type Nos. 06-3462C and 06-3463J can also be useo.

5.1.2 Contact Pitch

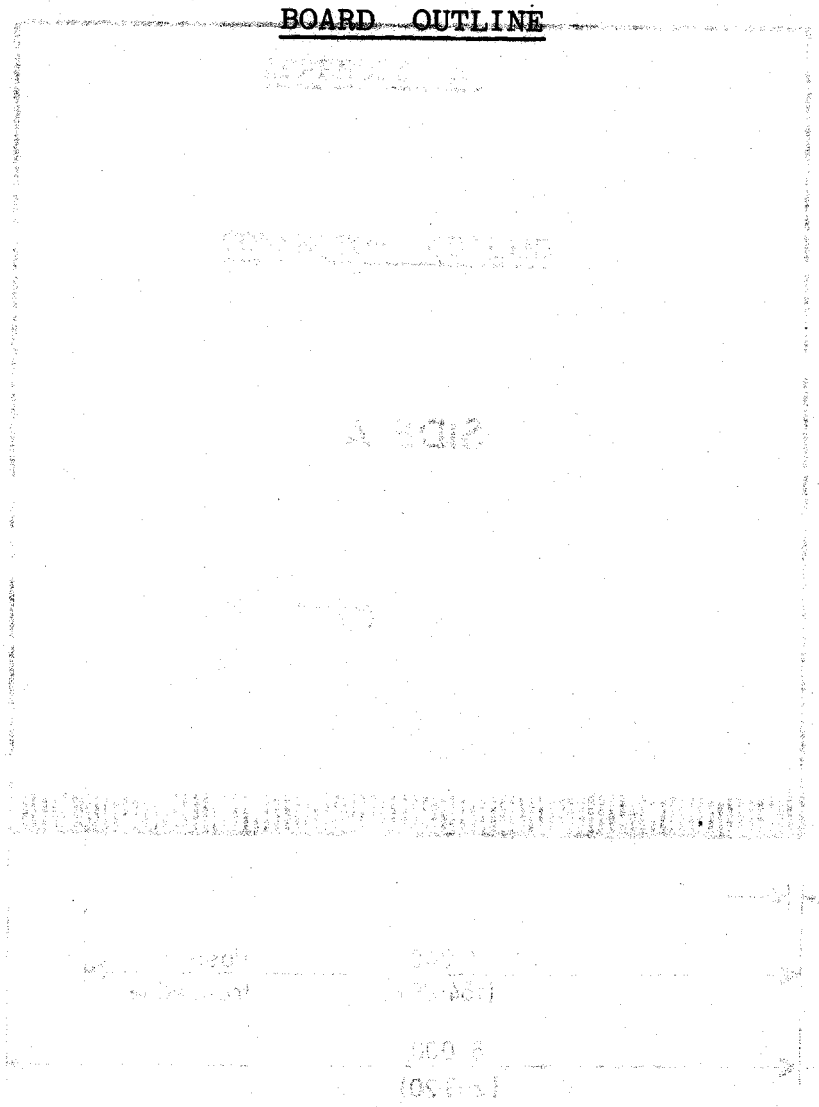
The contact pitch is 2.54 mm. 77 of the possible 78 ways are used, with a reference key 7 from the bottom (component side). The contacts used are on the solder side.

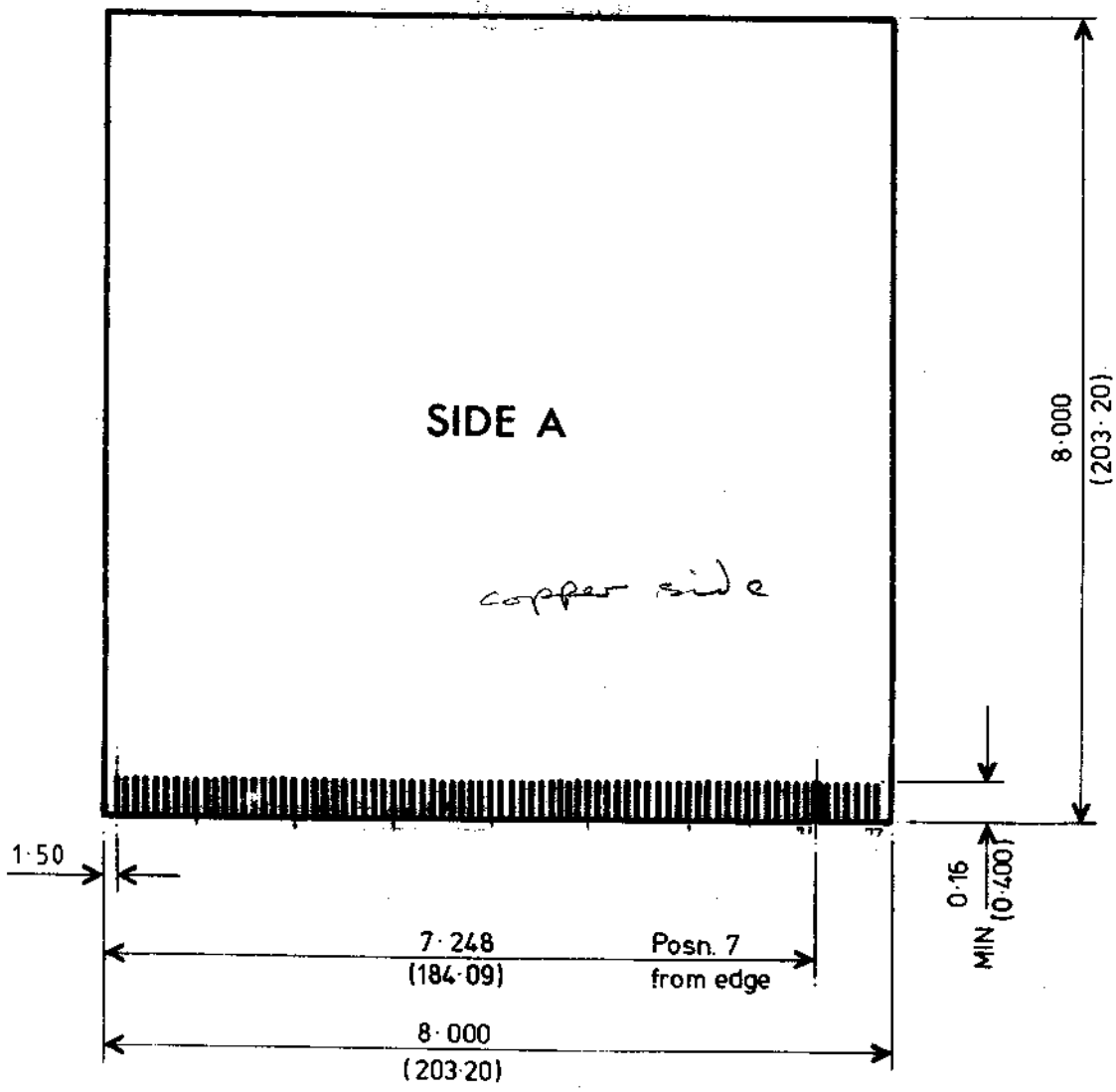
5.2. Connector Specification

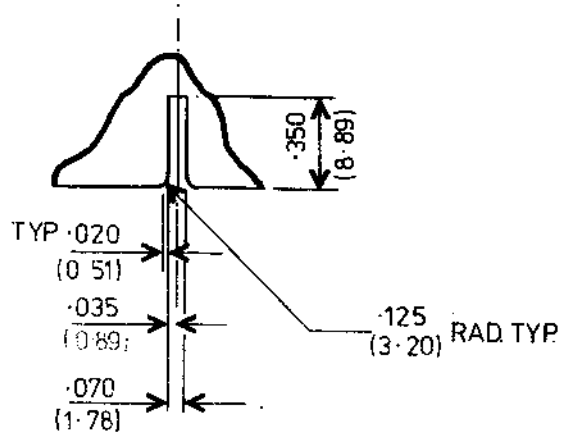
Suitable connectors are Vero type 14-0998G or Varelco type 00.6072-080-657-101 with polarising key at position 73, position 1 and 80 blank. (See Appendix B).

APPENDIX A

BOARD OUTLINE



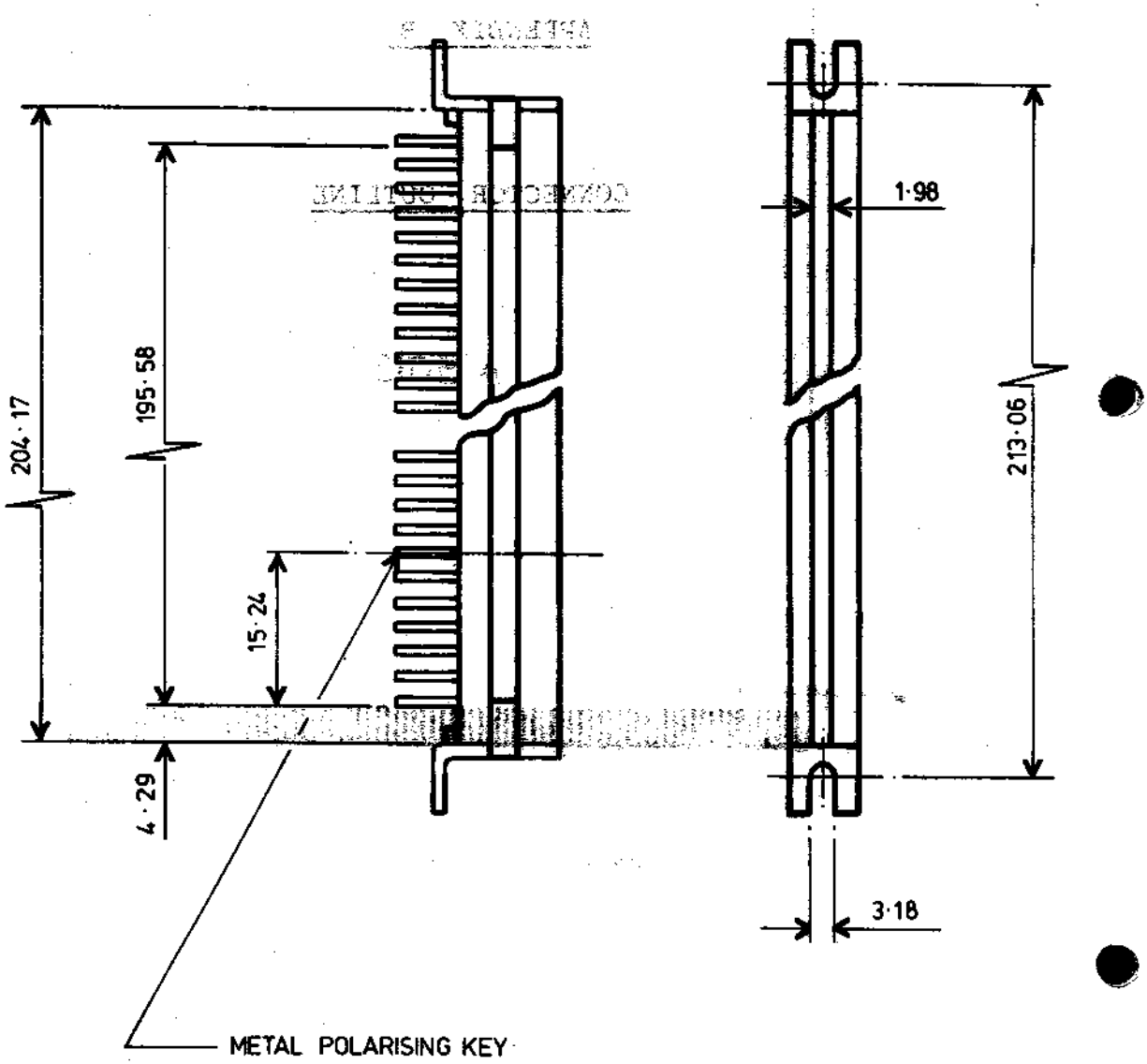




Detail of Polarising Key

APPENDIX B

CONNECTOR OUTLINE


204·17
195·58
15·24
4·29
1·98
213·06
3·18
METAL POLARISING KEY

APPENDIX C

NASBUS SUMMARY

Lines marked * are open collector: those overlined are $\overline{\text{NOT}}$ (logic level).

1,2,3,4	ØV: GROUND
5	Ø (buffered)
6,7,8	spare
9	$\overline{\text{RAMDISABLE}}$*
10	$\overline{\text{RESET SWITCH}}$
11	$\overline{\text{MEMEXT}}$
12	$\overline{\text{IOEXT}}$
13	$\overline{\text{DRIVE}}$ *
14	$\overline{\text{RESET}}$
15	$\overline{\text{HALT}}$
16	$\overline{\text{BUS AK IN}}$
17	$\overline{\text{BUS AK OUT}}$
18	$\overline{\text{BUS RQ}}$*
19	IEI
20	IEO
21	Reserved for $\overline{\text{NMI}}$
22	$\overline{\text{INT}}$*
23	$\overline{\text{WAIT}}$*
24	$\overline{\text{RFSH}}$
25	$\overline{\text{M1}}$
26	$\overline{\text{IORQ}}$
27	$\overline{\text{MREQ}}$
28	$\overline{\text{WR}}$
29	$\overline{\text{RD}}$
30	A0
31	A1
32	A2
33	A3
34	A4
35	A5
36	A6
37	A7
38	A8
39	A9
40	A10
41	A11
42	A12
43	A13
44	A14
45	A15
46,47,48,49	Reserved
50	D0
51	D1
52	D2
53	D3
54	D4
55	D5
56	D6
57	D7
58,59,60....65	Reserved
66,67	To separate signal and power lines
68,69	-ve 5V
70,71	-ve 12V
72	KEY
73,74	+ve 12V
75,76,77,78	+ve 5V