

G E M I N I
C O M P U T E R
S Y S T E M S

GM849/GM849A

FDC/SCSI BOARD

USER MANUAL

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1. Introduction

The Gemini GM849/GM849A is an 80-BUS compatible combined Floppy Disk Controller (FDC) and Small Computer Systems Interface (SCSI) board for use with Gemini MultiBoard systems.

In supporting floppy disk drives, the board has been designed to allow it to be used with up to eight mixed 8", 5.25", 3.5" or 3" drives. These may be single or double sided, ordinary or double track density drives, in single or double density formats. GM849/GM849A will also support the more recent high-density 5.25" drives that offer capacities of 1.2Mbytes (formatted) on a single floppy disk. Switching between the various modes and drives is entirely under software control. The board also has variable write precompensation and phase locked loop data recovery circuitry. The controller I.C. used is the Western Digital 2793.

In addition to floppy disk drive support the GM849 board offers support for hard (Winchester) disks and the later GM849A variant will also support tape streamers. The board does not contain the necessary circuitry to directly control the Winchester disk drives or tape streamers, but does provide a SCSI interface for connection of sub-systems. For example, the Gemini GM835 and GM885 Winchester sub-system series have been designed to plug directly into the GM849/GM849A's SCSI socket.

From a software point of view GM849/GM849A is NOT identical to the earlier GM809 FDC card, and GM829 FDC/SASI card. However the differences are minor and most current Gemini systems software automatically adjusts to match the type of board in use. Obviously some features of the later model cannot be supported on the earlier boards. (GM809 has no SCSI bus and no 8"/5.25" software switch. GM809/GM829 only support up to four floppy disk drives.)

Throughout this manual the term "GM849" will be used to apply to both the GM849 and GM849A variants, with any differences being explicitly stated.

1.1. Commissioning

Carefully unpack your GM849 and examine it for any mechanical damage. In the event of any damage please inform your dealer immediately. Your GM849 has been shipped to you fully tested and working and all that may be required is for the board to be plugged into the system. However, please take the time to read this manual as it may prove useful.

When plugging the GM849 into the bus, please take care. Excessive force should not be required. Any difficulty which may be encountered will, in all probability, be due to the keyway of the edge connector not fitting accurately into the slot in the edge of the board. Please ensure that the board is plugged in with the edge connector going in first and the correct way round. It is not possible to plug the board in incorrectly because of the keyway.

There are several linking options on the GM849. These have been set during manufacture and full details are provided in the section on links, to allow the user to configure the board to his own requirements. There are also several connectors for connecting drives and sub-systems, and these are described in the relevant sections.

2. Links

There are various link options on GM849, and these are set at manufacture by PCB tracks or shorting plugs. With these settings GM849 is directly usable in a normal 4MHz 80-BUS system and alternative settings should NOT normally be required. For non-standard systems the details of the various straps are given below.

NOTE: The default link settings are set either by shorting plugs or by sections of copper track on the underside of PCB between the appropriate pins of the link blocks. If an alternative setting is to be used this copper track will have to be cut to break the default connection. Once the track has been cut, a conventional push-on link can be used on the link block to select the required option, or a wire may be soldered from one pad to the other. Please take care, as an incorrect link may cause damage to the system, disk drives or GM849, and a poor connection will result in an unreliable system.

2.1. Link 1. (LK1.) TEST

This link option is not normally required by the user. It is located on connector J2, pins 4 and 5. The link should be installed during initial alignment of the board. Note that the link should be added AFTER the board has been powered up. Users wishing to use this option should obtain a copy of the Western Digital 2793 Data Sheet.

2.2. Link 2. (LK2.) 2793 Clock

In a standard 80-BUS system this link will not normally require changing.

LK2 is located on J1, pins 7, 8 and 9 (labelled a, b and c). (N.B. Some versions of the board may not have the "b" marked on the PCB.) This link is used to provide the necessary clock to the 2793 FDC chip. It determines whether the clock from the bus is passed straight to the 2793, or is divided by 2 first. The clock required by the 2793 is 2MHz.

Note that the source of the clock from the bus to this divider stage may be linked, via LK6, to be either the 80-BUS CLOCK line (line 5) or AUXCLK line (line 8).

When a 4MHz clock is supplied then it needs dividing by 2, and LK2 should be linked from a-b. This is the normal factory setting.

When a 2MHz clock is supplied then it does not need dividing further, and LK2 should be linked from b-c. The PCB track currently connecting a-b should be cut, and a new link made either with a soldered wire, or by adding a stripline connector and shorting plug.

2.3. Link 3. (LK3.) Write pre-compensation.

This link is used to enable/disable the GM849 write pre-compensation circuitry, and is located on J2, pins 1 and 2. This link will not normally require changing.

When the link is installed, write pre-compensation will automatically be activated on all floppy disk tracks beyond track 43 on any drive in double density mode, and this is the normal method of operation.

When the link is absent there will be no write pre-compensation. This option will only normally be required when initially aligning the board. In this situation the shorting plug may therefore be used to link LK1 (see above).

2.4. Link 4. (LK4.) SCSI /ATN line.

This link is located on J2, pins 7 and 8, and will not normally require changing. It is required for SCSI devices that require the /ATN signal on line 32 of the SCSI interface. The signal is present if the link is fitted, which it is normally via a PCB track on the underside of the PCB. If the signal is not required for any reason then this PCB track should be carefully cut.

2.5. Link 5. (LK5.) 80-BUS port address.

This link selects one of the two blocks of 80-BUS port addresses that the GM849 may occupy, and is located on J1, pins 1, 2 and 3 (labelled a, b and c). (N.B. Some versions of the board may not have the "b" marked on the PCB.) It will not normally need changing from its factory set state.

Linking a to b, the normal configuration, locates the board at ports E0-E7.

Linking b to c (and cutting the link a-b) locates the board at ports C0-C7.

Gemini software normally assumes that the board is located at ports E0-E7.

2.6. Link 6. (LK6.) Clock source selection.

This link determines the source of the clock used by the GM849, and is located on J1, pins 4, 5 and 6 (labelled a, b and c). (N.B. Some versions of the board may not have the "b" marked on the PCB.) It will not normally require changing from its factory set state. The clock source may be selected to be from either the 80-BUS CLOCK line (line 5) or the 80-BUS AUXCLK line (line 8). Link 2 then determines if this clock is then divided by 2 or not.

Linking a to b, the normal configuration, selects the 80-BUS CLOCK line.

Linking b to c (and cutting the link a-b) selects the 80-BUS AUXCLK line.

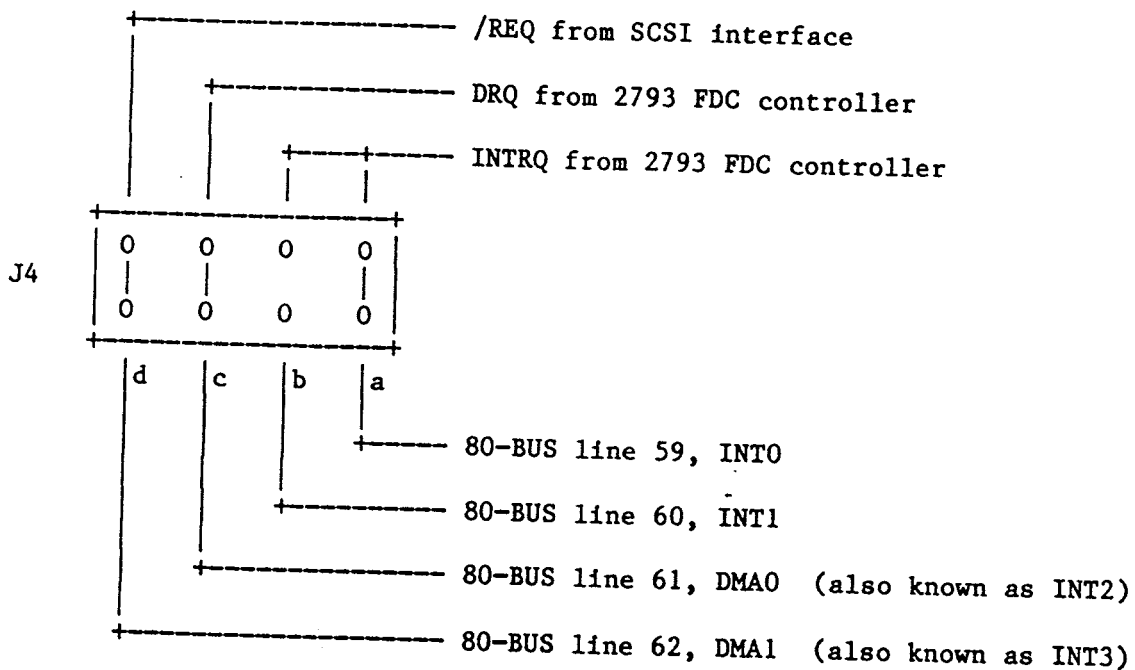
2.7. Ready line links

Connector J3 provides link options for drives without READY lines. You are referred to section 3.4, "Drives with no ready lines", below.

2.8. Link area J4 (GM849A ONLY)

There is an extra link area on GM849A boards only, for 80-BUS systems that use DMA disk operation. The links determine whether or not the GM849A outputs to the 80-BUS various support signals necessary for DMA operation. These 80-BUS lines are not normally used by Gemini MultiBoard cards and so these links, made by copper tracks, may normally be left as supplied. However, if you have specialised boards in your system that are already using these lines, then you should cut the copper tracks at J4.

Note that the INTRQ signal from the 2793 FDC controller is normally connected via link a to 80-BUS line 59, INTO. If this line is already in use, but line 60, INT1, is not, then cutting link a and inserting link b will move this signal to that alternative line.



2.9. Test points

There are various test and other signals also present on the J1 and J2 link strips. These are normally used for initial alignment of the board, when LK1 (TEST) will be set, and in this situation the signals have special purposes, as given in the square brackets [].

- TP1 - J2, pin 10 - Floppy WD (Write Data) signal [write precompensation]
- TP2 - J2, pin 9 - Floppy DIR (Direction) signal [VCO centre frequency]
- TP3 - J2, pin 6 - Floppy TG43 (track greater than 43) signal [Read Data pulse width]
- TP4 - J2, pin 3 - Ground
- D6 - J1, pin 10 - Currently unused control line

2.10. Board alignment

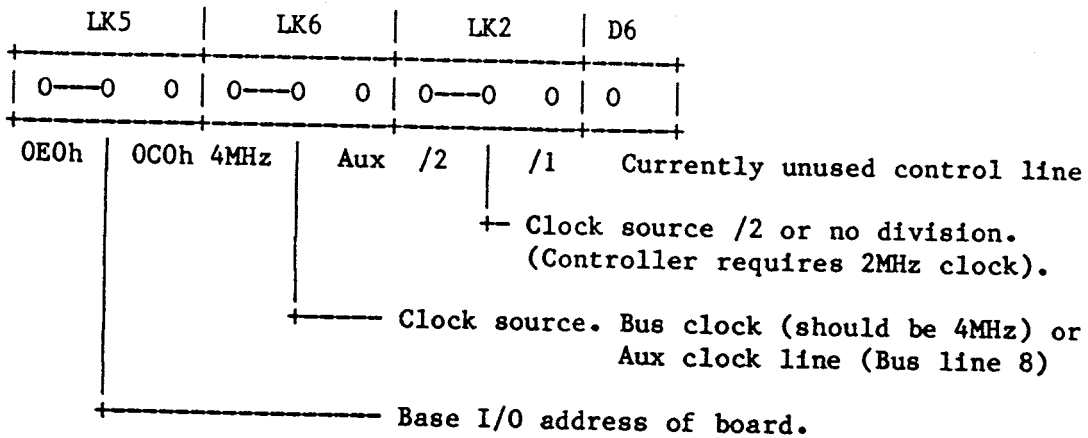
There are two variable resistors plus a variable capacitor on the GM849 board that are used to set up various parameters. These are set at manufacture and therefore it should not be necessary for the user to adjust them. However, the following notes are included for the sake of completeness of this documentation. Users requiring further details should obtain a copy of the Western Digital 2793 Data Sheet.

- a) apply power to the GM849
- b) remove the shorting plug from LK3 and install on LK1
- c) using VC1, adjust the VCO centre frequency on TP2 to 250KHz
- d) using VR2, adjust the positive read data pulse width on TP3 to 500nS
- e) using VR1, adjust the positive write precompensation pulse width on TP1 to 125nS
- f) remove the shorting plug from LK1 and reinstall it on LK3

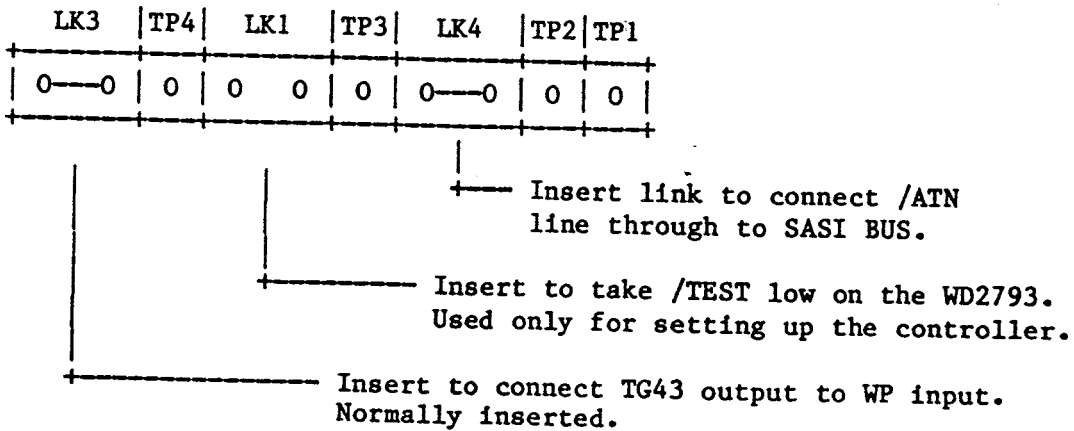
2.11. Link strip summary

The following diagrams summarise the link option and test point information given above for Link Strips J1 and J2.

2.11.1. Link strip J1



2.11.2. Link strip J2



3. Attaching floppy disk drives

3.1. Drive connectors

The GM849 is fitted with either 2 or 3 insulation displacement connectors for the connection of floppy disk drives, CONN 2 to CONN 4.

CONN 2 - is a 34-way right-angle connector for connecting up to 4 standard 5.25" (or smaller) floppy disk drives.

CONN 3 - is an optionally installed 34-way straight connector for connecting up to 4 further standard 5.25" (or smaller) floppy disk drives.

CONN 4 - is a 50-way straight connector for connecting up to 4 8" floppy disk drives.

The pin 1 end of each connector on the board is identified by a '1' on the PCB, and also with a triangular marking on the right-angle connectors. The pin 1 end of the cable assemblies will also usually be marked with a triangular marking on the connector, plus a striped cable. Ensure that the cable is connected with the correct orientation, or damage may occur to the board and drives.

The individual signals on the connectors are given in an Appendix.

3.2. Drive type

The GM849 design is capable of controlling a wide variety of drive types, provided that their interfaces are compatible with that shown in the Appendix.

The following drives have actually been used by Gemini, and are therefore known to be compatible with GM849. (Note that this assumes that correctly configured software is being used.)

Drive type	Size	TPI	Sides	Special notes
Epson SD540	5.25"	96	2	
Epson SM140	3.5"	135	2	
Matsushita EME101	3"	100	1	
Micropolis 1115F-V	5.25"	96	1	Linked as "standard" i/f
Micropolis 1115F-VI	5.25"	96	2	Linked as "standard" i/f
Mitsubishi M2896	8"	48	2	
Pertec FD250	5.25"	48	2	See note (c) below
Teac FD35F	3.5"	135	2	
Teac FD55B	5.25"	48	2	
Teac FD55F	5.25"	96	2	
Teac FD55GF	5.25"	96	2	Dual speed drive
Toshiba ND-04D	5.25"	48	2	
Toshiba ND-06D	5.25"	96	2	

There are certain other drives that are not completely compatible with the standard GM849 drive interface, but which may still be used provided that certain conditions are observed.

e.g.

a) Micropolis 1015F-V and 1015F-VI drives use line 6 of the drive interface (normally the fourth drive select line) as the drive Ready line (instead of line 34). These drives may still be used, provided that:

- i) none of them are set to physical address 3 (or "7")
(as the line used is really the Ready line)
- ii) no other drive is set to physical address 3 (or "7")
(as the Micropolis drive is going to activate this via its Ready line)
- iii) the relevant "ready" link(s) on J3 are installed (see below)
(as the 1015 drive's actual "Ready" will not be seen by GM849).

b) Micropolis 1115F-V and 1115F-VI drives may be linked one of two ways; the same way as 1015 drives (as described above) or as "standard" drives. If used in 1015 mode, then the points in a) apply. To link an 1115 as "standard" move link W6 to position W8 and move link W17 to position W34.

c) Pertec FD250 drives do not have a Ready line. The relevant link(s) must therefore be installed in J3 (see below).

3.3. Drive link options

There are a variety of link options available on most drives. The ones of most relevance here are the termination links/resistors and the address selection. These points are covered below. Other drive link options are beyond the scope of this manual, and they are not discussed further.

3.4. Drives with no "Ready" line

GM849 assumes that any drive connected to it provides a "drive ready" signal on pin 34 (CONN2 or CONN3) or pin 22 (CONN 4). If the particular make of drive used does not generate such a signal, then links should be inserted in Link Block J3, as shown in the diagram below. With a link installed, a "drive ready" signal is automatically generated whenever that drive is addressed.

GM849 Drive Number:

3 0 1 2 7 4 5 6

J3 identification:

	0	1	2	3	4	5	6	7
J3	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

Insert links as appropriate

3.5. Drive address selection

Up to eight floppy disk drives in total may be connected to the GM849, and these may be 3", 3.5", 5.25", 8" or various combinations of these.

The standard design of floppy drive interface can only support up to four drives in total, and so on GM849 various elements of the design are duplicated to allow this higher number of drives to be controlled.

Up to four 3", 3.5" or 5.25" drives in total may be installed via CONN 2 (34-way), and up to four 8" drives may be installed via CONN 4 (50-way). In certain circumstances more than four 5.25" (or smaller) drives may be required, and for this purpose CONN 3 needs to be installed.

NOTE: CONN 3 (34-way) is basically connected in parallel with CONN 4 and so should be considered as being the same connector as regards selecting drive addresses; thus each drive that is added via CONN 3 reduces the number of 8" drives that can be connected to CONN 4, and vice versa.

To summarise the number of drives that may be used on GM849:

$$(\text{Number of 3" + 3.5" + 5.25" on CONN 2}) \leq 4$$

$$(\text{Number of 3" + 3.5" + 5.25" on CONN 3}) + (\text{Number of 8" on CONN 4}) \leq 4$$

3.6. Drive references

Gemini CP/Ms of BIOS 3.4 or greater can support GM849. With these BIOSs it is necessary to give the BIOS a reference number (via the relevant .CFG file(s)) for each physical drive present, to indicate the physical address of that drive (set by a link on the drive). Users writing their own software drivers for GM849 should also refer to the sections in this manual on Software Interface and GM829/GM849 Compatibility.

Logical BIOS 3 ref. (in .CFG file)	Physical Drive address (set by link)	GM849 Connector (CONN)
0	0	2
1	1	2
2	2	2
3	3	2
4	0	3 or 4
5	1	3 or 4
6	2	3 or 4
7	3	3 or 4

3.7. Drive termination

The last floppy disk drive on each drive cable (34 or 50-way) should be fitted with line termination resistors; all other drives should have the termination resistors removed and stored in a safe place in case they are required in the future.

4. Software

Gemini Computer Systems supplies, via its dealers, both the CP/M-80 and CP/M-86 Operating systems for use with Gemini MultiBoard systems fitted with the GM849 FDC/SCSI board, located at ports E0-E7h. Note that no Gemini software is available for Nascom based systems fitted with GM849.

4.1. CP/M-80

There are two variants of CP/M-80 (Version 2.2) available for use with MultiBoard systems using the GM849 controller board, referred to as GM512 and GM555. For GM849 these must be BIOS 3.4 or later, and for GM849A, BIOS 3.5 or later.

The GM512 package is for systems using a 48 tpi floppy disk drive as the base drive, and the GM555 package is for systems using a 96 tpi floppy disk drive as the base drive. (Note that both versions do allow a wide variety of different drives to be supported by modifying user-configurable files, but you must first of all obtain a version that can be "booted" on your main drive.)

If you are already using Gemini systems based on the GM809 or GM829 boards you must take care to ensure that none of the CP/M Operating Systems supplied with, or purchased for use with those systems, are used with any systems using the GM849 board, as this will result in incorrect operation.

Please note that Digital Research Inc, the suppliers of the CP/M Operating System, only grant a license that states that each CP/M may only be used on a SINGLE computer system at a SINGLE site, and a separate CP/M must be purchased for each and every system that is to run CP/M.

4.2. CP/M-86

For systems that also incorporate the Gemini GM888 8088 processor board, the Gemini GM578 CP/M-86 package is available. When ordering this package for use with a system containing GM849 you must ensure that you specify that they must contain Gemini BIOS version 0.3 or later, as earlier releases did not support the GM849 board.

4.3. RP/M

Gemini GM811 and GM813 Z80 CPU boards may be fitted with the RP/M ROM monitor program. All versions of RP/M are compatible with GM849 for "booting" the relevant CP/M (see above) from a floppy disk drive. However RP/M will not "boot" a Winchester hard disk drive, regardless of controller board type.

4.4. SIMON

Gemini GM811 and GM813 Z80 CPU boards may already be fitted with the SIMON (Simple MONitor) ROM program. All versions of SIMON are compatible with GM849 for "booting" the relevant CP/M (see above) from a floppy disk drive. However, to "boot" a Winchester hard disk drive via a GM849 board, SIMON must be of version 4.0 or later. With GM849A it must be of version 4.2 or later.

5. Circuit Description and Software Interface

To the host 80-BUS system the GM849 appears as a block of 8 Input/Output ports. By default these ports occupy the addresses E0-E7 (hexadecimal), although a 'cut-and-strap' option is provided on the board for the addresses to be changed to C0-C7. (See the section on links above.) Thus, with appropriate software, two GM849 boards may be used in a single system. The allocation of the ports is as follows:

Port	Read	Write	
E0	Status register	Command register)	Internal 2793 registers
E1	Track register	Track register)	
E2	Sector register	Sector register)	
E3	Data register	Data register)	
E4	External status reg.	Drive select reg.	
E5	SCSI control lines	SCSI control port	
E6	SCSI data bus	SCSI data bus	
E7	----- do not use-----		

Details of the commands and usage of the WD2793 disk controller can be found in the appropriate Western Digital disk controller data sheet (not supplied). Similarly details on commands and usage of the Winchester Controller may be found in the appropriate user manual.

5.1. Winchester drives.

The implementation of the SCSI bus allows Winchester Controller boards such as the Xebec SI410 or Western Digital WD1002 to be interfaced to GM849. The full SCSI specification is given in an ANSI standard, but descriptions of the relevant subset can be found in the user manuals for the various SCSI based Winchester controllers.

5.2. SCSI interface

SCSI ports - Data Bus (port E6)

Data Bus READ (RD on port E6).

Reads data directly from the external SCSI data bus.

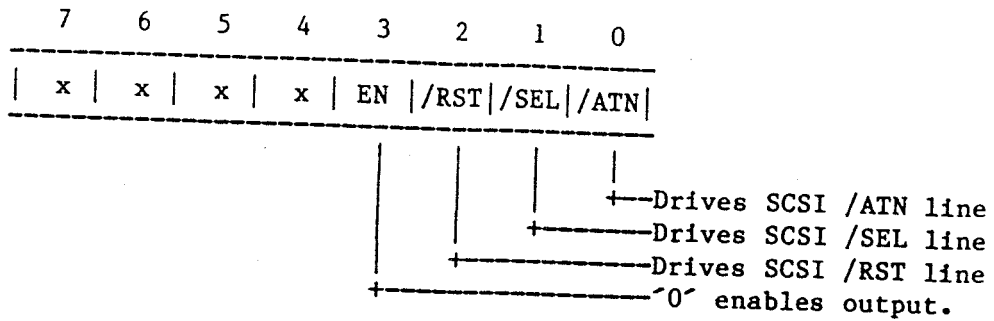
Data Bus WRITE (WR on port E6).

Writes data to an on-board latch. If bit 3 of port E5 is 0 (see below), and the SCSI control line I/O is high, then the outputs of the latch are enabled on to the SCSI data bus.

NB A READ or WRITE of the data port automatically generates an /ACK signal on the SCSI bus at the end of the Z80 read/write cycle if SCSI control line /REQ is low.

SCSI ports - Control port (port E5)

WRITE



Notes: With GM849 bits 0-2 directly drive the appropriate SCSI line. They are only active for the duration of the write cycle.

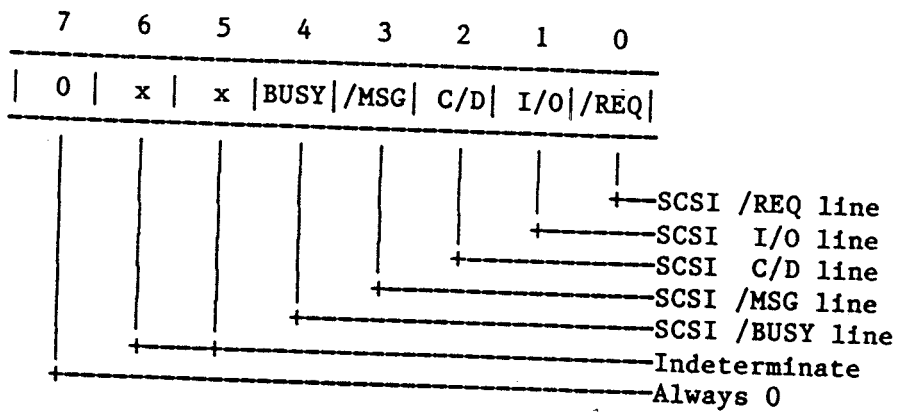
With GM849A bits 0-2 are latched.

Bit 3 is latched. It should normally be set to 0, but should be set to 1 if control is to be passed to another bus master on the SCSI bus.

Bits 4-7 may be either 1 or 0.

With GM849 (but NOT with GM849A) the SEL line is only active for the duration of the Z80 write cycle. The resultant 'pulse' select signal, while it does not meet the SCSI specification, is perfectable acceptable to many SCSI controllers (eg Xebec S1410). This point should be checked in the user manual of any SCSI controller board that is intended to be used in conjunction with GM849.

READ



Bit

7 is always 0. It can be used to distinguish between GM849 and the earlier GM829 disk controller board. With GM829 this bit is always a 1. GM829 has an identical SCSI interface, but there are small differences in the floppy disk interface. (It uses a WD1797 controller, and there is a difference in the action of the disk drive address latch).

6 may be a 1 or a 0.

5 may be a 1 or a 0.

4)

3) These are direct representations of the appropriate

2) SCSI control lines.

1)

0)

5.3. Floppy drives

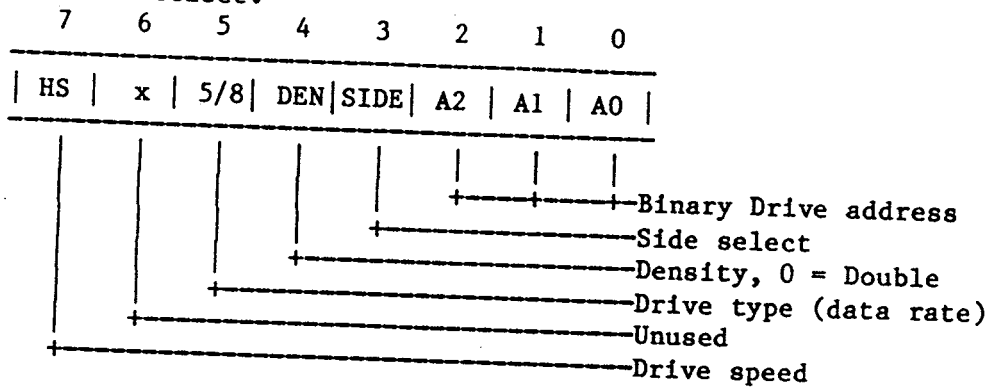
GM849 utilises the Western Digital WD2793 floppy disk controller integrated circuit as the basis of its floppy disk interface. In addition a small amount of additional support logic provides direct support for up to eight floppy disk drives, with software control of various parameters of the subsystem interface.

Floppy Disk Ports.

E0-E3 address the four internal registers of the WD2793.

Port E4

WRITE - Drive select.



Bit

- 7 is connected to pin 2 on the disk interface connector. With modern high-density drives such as the TEAC FD55GF this controls the rotational speed of the drive. It is set to '1' for the high density option, '0' otherwise.
- 6 may be a 1 or a 0.
- 5 is connected to the 5/8 control on the WD2793. This is usually set to '0' for 5.25" drives, and '1' for 8" drives. It actually sets the data transfer rate of the disk interface. (For double density this is either 500kpbs = 8" (or 5.25" if high-density drive, see bit 7 above) - or 250kpbs = 5.25". For single density the rates are halved).
- 4 This selects the data recording technique to be used. '0' represents MFM (double density), and '1' represents FM (single density).
- 3 Selects the appropriate side of a double sided drive. Set to '0' for side 0, '1' for side 1.
- 2)
- 1) hold the binary address of the selected drive.
- 0) Addresses in the range 0-3 select a drive connected to connector 2, while addresses in the range 4-7 are routed to connectors 3 and 4.

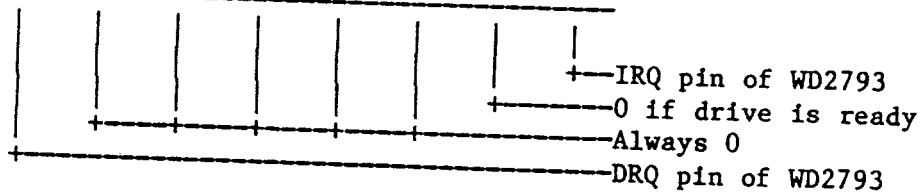
Connectors 3 and 4 are connected in parallel, connector 4 being a conventional 50-way 8" interface, and connector 3 being a conventional 34-way 5.25" interface. Thus, the connectors offer direct connection for 8 drives connected via standard 34-way connectors, or 4 by a 34-way and 4 by a 50-way connector.

Note: Any write to this port triggers/retriggers the monostable that generates the 'motor-on' signal to the floppy disk drive. When this monostable is first triggered there will be an initial delay of about one second before READY (see below) becomes true. This delay is introduced to allow the floppy disk to come up to speed. The 'motor on' signal will remain active until the time-out period expires without a write occurring to the drive address port. This period is about four seconds. (i.e. after four seconds of floppy disk inactivity the drives will stop rotating. This is done to reduce noise levels and wear-and-tear on the drives and media).

Port E4

READ - External status

7	6	5	4	3	2	1	0
DRQ	0	0	0	0	0	/RDY	IRQ



Bit

- 7 is a Data Request from the WD2793
- 6)
- 5)
- 4) These are always 0
- 3)
- 2)
- 1 is '0' if the attached drive is ready, is a '1' otherwise. This signal is gated with the 'motor on' signal from the card.
- 0 is an Interrupt Request from the WD2793

6. GM829/GM849/GM849A Compatibility

6.1. GM829/GM849 software compatibility

The GM849 FDC/SCSI board is broadly compatible with the earlier GM829 FDC/SASI board. The following notes outline those areas in which the two boards are different. Because of the "board type" bit (as described in (a) below) it is possible to write drivers that are capable of determining whether the board is GM829 or GM849, and then act accordingly.

- a) Bits 7, 6 and 5 on the SCSI status port (OE5h) are now no longer wired to a logical 1. Bit 7 will always return 0 (to allow auto determination of GM829 or GM849), and bits 6 and 5 are indeterminate.
- b) In order for the GM849 SCSI interface to enable data onto the SCSI bus at the appropriate time, bit 3 of the SCSI control port (OE5h) must always be 0.
- c) GM849 uses a WD2793 as its integrated FDC controller rather than the 1797 used on the GM809 and GM829 boards. With the xxx3 variation of the FDC chip the drive side selection is done externally to the controller, and as a result a small change is necessary to the READ/WRITE commands used previously. Bit 3 in the drive address latch is now used for side selection.
- d) The drive address of the floppy drive is now binary encoded in a three-bit field - up to eight drives are now supported, and the decoding is done in hardware on the GM849 board. For loose compatibility with GM829 (so that previous software will still "boot" the floppy) an address of 1 selects drive 0, side 0, and the other addresses are shifted accordingly:

BIOS Drive Ref.	GM829 Software Address	GM849 Software Address	Physical Drive address GM829	Physical Drive address GM849
0	0001 (1)	001 (1)	0	0 - CONN 2
1	0010 (2)	010 (2)	1	1 - CONN 2
2	0100 (4)	011 (3)	2	2 - CONN 2
3	1000 (8)	000 (0)	3	3 - CONN 2
4		101 (5)		0 - CONN 3 or 4
5		110 (6)		1 - CONN 3 or 4
6		111 (7)		2 - CONN 3 or 4
7		100 (0)		3 - CONN 3 or 4

6.2. GM849/GM849A software compatibility

With GM849A bits 0-3 (/ATN, /SEL, /RST and EN) of the SCSI Control port (port E5) are latched, whereas on GM849 only bit 3 (EN) is latched, and bits 0-2 directly drive the appropriate SCSI line (i.e. they are only active for the duration of the write cycle).

For code that is compatible with both GM849 and GM849A it should be written to assume that these lines are all latched, and that the software should clear them as well as setting them. In the case of GM849A this will obviously function correctly, whilst in the case of GM849, the "clear" will serve no purpose, as the line will already be cleared.

6.3. GM849/GM849A hardware compatibility

If you have a GM849 and you require the additional features of the GM849A, then some of these can be made relatively simply by modifying the GM849. Note that making these modifications will invalidate the warranty on your GM849.

- a) The GM849A has the MOTOR ON signal connected to the 50 way 8" drive connector (CONN 4). To do this on GM849 connect a wire link from the plated through hole adjacent to CONN 4, and marked P4, to pin 4 of CONN 4.
- b) Whilst GM849A has all three of bits 0-2 (/ATN, /SEL, and /RST) of the SCSI Control port (port E5) latched, whereas GM849 has none, it is only bit 1, /SEL, that is relevant to allow a number of alternative SCSI controllers (both Winchester and tape streamer) to be interfaced to the GM849. GM849 may be modified to latch bit 1 without the addition of any components, but by cutting various tracks and adding extra links. Details of these modifications are available via your dealer on request.

Note that when this modification has been made the software used must be that for GM849A, and as noted under "Software Compatibility" above, the fact that all of the bits are not latched will be transparent to the software.

- c) The extra lines for possible DMA operation, as detailed in section 2.8, may be added by taking the relevant signals to the 80-BUS via spare elements of the 74LS244 buffer, IC28.

A. Connector Details

CONN 1 - 50-way Connector

CONN 1 is provided for the connection of SCSI devices.

2	Data 0
4	Data 1
6	Data 2
8	Data 3
10	Data 4
12	Data 5
14	Data 6
16	Data 7
18	No connection
.	" "
.	" "
30	" "
32	/ATN
34	No connection
36	/BUSY
38	/ACK
40	/RST
42	/MSG
44	/SEL
46	C/D
48	/REQ
50	I/O

All odd pins (1-49) are Grounds

Line 32 may be disconnected (if not required) via LK4

CONN 2 and CONN 3

CONN 2 and CONN 3 are provided for the connection of 5.25" (or smaller) drives.

2	/SPEED	For dual-speed drives
4	N.C.	No connection
6	/DS3	Drive Select 3
8	/IP	Index pulse
10	/DS0	Drive Select 0
12	/DS1	Drive Select 1
14	/DS2	Drive Select 2
16	/MTRN	Motor On
18	/DIR	Direction Select
20	/STEP	Step
22	/WD	Write Data
24	/WG	Write Gate
26	/TROO	Track 00
28	/WPRT	Write Protect
30	/READ	Read Data
32	/SIDE	Side Select
34	/RDY	Drive Ready

All odd pins (1-33) are Grounds

CONN 4 - 50-way connector

CONN 4 is provided for the connection of 8" drives.

2	/TG43	Track greater than 43
4	(/MTRN)	(Motor on - GM849A only)
6	N.C.	No connection
8	N.C.	No connection
10	N.C.	No connection
12	N.C.	No connection
14	/SIDE	Side Select
16	N.C.	No connection
18	N.C.	No connection
20	/IP	Index pulse
22	/RDY	Drive Ready
24	N.C.	No connection
26	/DS0	Drive Select 0
28	/DS1	Drive Select 1
30	/DS2	Drive Select 2
32	/DS3	Drive Select 3
34	/DIR	Direction Select
36	/STEP	Step
38	/WD	Write Data
40	/WG	Write Gate
42	/TROO	Track 00
44	/WPRT	Write Protect
46	/READ	Read Data
48	N.C.	No connection
50	N.C.	No connection

All odd pins (1-49) are Grounds