The Gemini MultiBoard Microsystem

SERIAL I/O

DAUGHTER BOARD

INSTRUCTION MANUAL

GM 818
Issue 1
2-02-84

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1. INTRODUCTION

1.1. The Gemini GM818

The Gemini GM818 is a dual channel serial I/O Daughter Board designed to be attached 'piggy-back' fashion to the GM816 I/O card. It provides two independently controlled, fully programmable serial interfaces, each with full modem control and its own baud rate generator. There are also four spare user-definable TTL outputs available, and two user-readable inputs.

Connections between each UART and its DB25 connector may be cut and relinked at the points provided to accomodate alternative RS232 configurations. As supplied the GM818 is linked to Gemini Galaxy configuration.

1.2. Guarantee

Your GM818 Serial I/O board is guaranteed by the supplier (your Dealer) for one year from the date of purchase. However, being a system module, any faults attributable to incorrect implementation of the board within your system will be fully chargeable as to both parts and labour.

Any queries regarding the implementation of your GM818 Serial I/O board should be directed at your Gemini dealer.

1.3. Pre-Installation Notes

Carefully examine your GM818 for any damage that it may have suffered in transit. In the event of any damage please inform your dealer immediately.

Packed with your GM818 you should find:-

* 1 x 50 way cable (about 2.5 inches long)
* 4 x 4BA 1 inch screws, nuts and shake-proof washers
* 4 x .75 inch mounting pillars

Before attaching the board to the GM816 it may prove useful to read through the section of this manual on PL1/2 link options as these can only be successfully altered with the GM818 on a flat surface.

2. LINK OPTIONS

There are a variety of link options available on the GM818. This section describes these options.

2.1. Port addresses

The GM818 board uses two 8250 type UARTs and occupies 16 (10H) consecutive Z80 I/O ports. These may be link selected to any 16 port boundary.

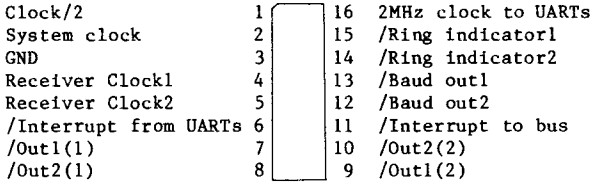
The Chip Select decode pin (CS) is located near pin 50 of the 50-way connector on the GM818. This pin should be linked to one of the fifteen port select signals (PS0-PSE) brought onto the daughter board via the 50-way connector.

As shipped, 'CS' is linked to the plated-through hole numbered '28'(PS A). This 16-port decode from the GM816 is further decoded to give two 8-port decodes, X0 to X7 and X8 to XF, as each 8250 UART requires 8 ports. Thus, as supplied, the GM818 is set so that UART1 occupies ports A0-A7, and UART2 occupies ports A8-AF.

It should be noted that if you are using a Gemini CP/M and wish to use one of the UARTs on the GM818 as the CP/M list device instead of the one on the CPU board, then a base port address of 80H or higher must be used. Note that the Gemini CP/M will ONLY initialise the 8250 UART on the CPU board. A separate program must be run to initialise the UARTs on the GM818 board. Demonstration examples are given later in this manual.

2.2. LKB 1

LKB1 is a 16-pin header plug on the GM818 allowing user selection of clock rate and interrupts, giving access to the /OUT1 and /OUT2 user-designated outputs and the Ring Indicator inputs, and also allowing connection of an external Receiver Clock to either or both of the Baud Out outputs.



2.2.1. Clock

The 8250 UARTs are run from a 2MHz master clock. If the system clock is running at 2MHz then pin 2 of LKB1 should be chosen as the UART clock rate and linked across to pin 16. A system clock of 4MHz will require division by 2 before it is connected to the UARTs. In this case pin 1, which is the system clock divided by 2, should be linked to pin 16.

2.2.2. Baud Rate

The Receiver Clock inputs to the two 8250 UARTs are brought out to LKB1 so that they may or may not be linked to the Baud Out outputs. If an external receiver clock is used then it should be linked to the appropriate Receiver Clock input. Normally Baud Out is connected to Receiver Clock.

2.2.3. Interrupts

UART interrupts can be taken to the system bus by linking pin 6 to pin 11 of LKB1. Reading the Interrupt Identification Registers will show which UART is causing the interrupt. As the 8250 is not of the Z80 family, if Vectored Interrupts are used pin 6 will have to be taken to a bit of a PIO or the CTC, these chips then sending the Interrupt Vector.

If the Ring Indicator pin is connected to a MODEM then an Interrupt may be generated if the phone rings. Alternatively the ring indicators may be used as general purpose inputs. An example of an alternate use would be as on the GM811 and the GM813 CPU boards. Here, the Ring Indicator input is taken low by an on-board link and can be read on power-up via the MODEM Control Register to determine whether or not the CPU board should be set up to act as a terminal.

2.2.4. User Outputs

The User Outputs are user-definable bits within the UART and may be caused to change state by a user program. An example of use on the Gemini CPU boards is to switch between RS232 and Cassette output functions. There are two user-designated outputs per 8250 UART.

2.2.5. LKB1 Pin Descriptions.

The following is a pin oy pin description of LKB1.

Name	Pin	Desription
Clock/2	1	System clock divided by 2 (normally 2MHz).
System clock	2	Clock from pin 5 of the 80-BUS (normally 4MHz).
Receiver	4	This input is for the 16x baud rate clock for the Clock receiver section of UART1. In some cases it may prove useful to have the Receiver Clock connected to an external source. Normally this input is taken from Baud out.
Receiver Clock	5	As pin 4 but for UART2.
/Int from UART	6	Linking this pin across to pin 11 enables interrupts to reach the bus. Note that as the 8250 is not of the Z80 family, vectored interrupts can only be handled if the interrupt line is taken to a bit of a PIO or the CTC.
/Out1(1) /Out2(1)	7 8	User-designated output that can be set to an active low by programming bit 2 of the MODEM Control Register to a high level. The Out1 signal is set high on reset.
/Out1(2) /Out2(2)	9 10	As Out1 but bit 3 of the MODEM Control Register.

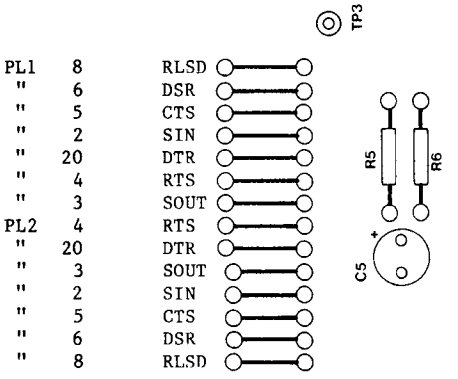
/Baudout2	12	
/Baudout1	13	16x clock signal for the transmitter section of the 8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The GM818 is shipped with baudout linked to receiver clock.
/Ring Indicator2	14	
/Ring Indicator1	15	When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The /RI signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the /RI input has changed from a high to a low state since the previous reading of the MODEM Status Register. NOTE: Whenever the RI bit of the MODEM Status Register changes from a high to a low state an interrupt is generated if enabled.
Clock to UARTs	16	This pin takes the 2MHz clock to the UARTs.

2.3. PL1/PL2 Link Options

If you already own or have access to other RS232 interfaced equipment and find that PL1 and PL2 on the GM818 do not match the pin configuration you are currently using then you may relink the GM818 sockets to your own configuration using the tracks provided.

All connections between PL1 and 2 and the RS232 drivers/receivers are taken through links (marked sections of copper track) which may be cut, using a sharp knife or a hand-held drill bit rotated slowly until the copper is removed, and re-linked to the desired configuration.

Cutting these links will not affect the guarantee given by your Dealer providing only tracks designated as 'user-removable' are removed. The circuit diagram clearly shows connections from UARTX to PLX.



3. INSTALLATION

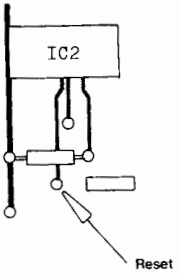
3.1. Mounting the GM818

Push either end of the 50-way cable onto the matching plug on the Daughter Board. Now, with the component side of the GM818 facing up, attach the other end of the cable to the 50-way plug on the GM816. The four holes on each board should now line up and the two boards can be secured in this position with the screws, pillars, washers and nuts provided.

3.2. Linking the Reset Pin

The 8250 UARTs are automatically reset on power-up, but they are not affected by the system reset line. If you wish to have the UARTs reset when the system is reset then a wire link will have to be fitted.

On one of the shorter edges of the board you will find a pin marked 'TP1'. This can be linked to the system reset line by taking a wire below to a specific plated-through hole on the GM816, as illustrated below. Resetting the 8250 will clear the control logic and all registers except the Receiver Buffer, Transmitter Holding register and Divisor Latches.



4. RS232 INPUT/OUTPUT SIGNALS

The RS232 Input/Output signals for UARTs 1 and 2 are provided on the two DB25 connectors, labelled PL1 and PL2 respectively. The following descriptions apply to the signals at PL1 and PL2 on the standard GM818 configuration.

SIN (Serial Input) Pin 2
Serial data input from the communications link (peripheral device, MODEM, or data set).

SOUT (Serial Output) Pin 3
Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Spacing (logic 0) state upon reset.

RTS (Request to Send) Pin 4
When high, informs the MODEM or data set that the 8250 UART is ready to transmit data. The RTS output signal can be set to an active high by programming bit 1 (RTS) of the MODEM Control Register. The RTS signal is set low upon reset.

CTS (Clear to Send) Pin 5
The CTS signal is a MODEM Control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register.
NOTE: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

DSR (Data Set Ready) Pin 6
When high, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the 8250 UART. The DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR input has changed state since the previous reading of the MODEM Status Register.
NOTE: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

RLSD (Received Line Signal Detect) Pin 8
When high, indicates that the data carrier has been detected by the MODEM or data set. The RLSD signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the RLSD input has changed state since the previous reading of the MODEM Status Register.
NOTE: Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

DTR (Data Terminal Ready) Pin 20
When high, informs the MODEM or data set that the 8250 UART is ready to communicate. The DTR output signal can be set to an active high by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set low upon a Master Reset operation.

5. THE 8250 UARTs

The following tables describe the functions of the registers of the 8250 UARTs. Note that the 'x' in the port number will depend on what base address has been selected for the GM818 board. This will normally be A0H. The first port number given corresponds to UART1 and the second to UART2.

Line Control Register (port x3/xB read/write)

Bits 0 and 1 determine the number of bits in each transmitted or received character:

Character Length	Bit 1	Bit 0
5 bits	0	0
6 bits	0	1
7 bits	1	0
8 bits	1	1

Bit 2 determines the number of stop bits in each character. If a logic 1, 1.5 stop bits for a 5 bit character, 2 stop bits for the 6, 7 and 8 bit character lengths. If a logic 0, 1 stop bit whatever the character length.

Bit 3 parity enabled when logic 1, causes parity generation on transmit and verification on receive.

Bit 4 parity select, logic 0 for odd parity, logic 1 for even parity. Odd parity means that the character will have an odd number of ones. Even parity means the character the character will have an even number of ones.

Bit 5 stick parity, inverts the effect of bit 4.

Bit 6 set break, when logic 1 the serial output from GM818 is forced to the spacing state, i.e. negative. This is irrespective of transmitter activity.

Bit 7 DLAB bit, this bit is used to switch ports x0/x8 and x1/x9 between the receive/transmit buffers (x0/x8), the interrupt enable register (x1/x9), and the baud rate divisor registers. When logic 1 the divisors are accessible and when logic 0 the receive/transmit buffers and the interrupt enable register are accessible.

Line Status Register (port x5/xD read/write)

Bit 0 Data Ready indicator, logic 1 whenever a complete character has been received and is ready to be read. Reset either by a read of the receiver data register or by writing a 0 to this location.

Bit 1 Overrun Error indicator, set to logic 1 if the Receiver Buffer was not read prior to the current character being loaded in. Reset by a read of the Line Status register.

Bit 2 Parity Error indicator, set if a parity error is detected. Reset by a read of the Line Status register.

Bit 3 Framing Error, set if the received character did not have a valid stop bit. Reset by a read of the Line Status register. This is the most common type of error from tape interfaces.

Bit 4 Break Interrupt indicator, set to a logic 1 whenever the serial input to GM818 is held in spacing (-12 volts) for longer than a full character period.

Bit 5 Transmitter Holding Register Empty indicator, set to a logic 1 whenever the Holding register is ready to accept a new character. Reset by loading the Transmitter Holding register (port x0/x8).

Bit 6 Transmitter Shift Register Empty indicator, set to a logic 1 whenever the Transmitter Shift register becomes empty. Reset by the Transmitter Shift register becoming active. This bit is read only.

Bit 7 There is no bit 7. This location is permanently set to logic 0.

Modem Control Register (port x4/xC read/write)

Bit 0 DTR output, set to logic 1 to set the DTR output from GM818 positive. Reset to take the DTR output negative.

Bit 1 RTS output, set to logic 1 to set the RTS output from GM818 positive. Reset to take the RTS output negative.

Bit 2 OUT 1 output. This bit controls the OUT1 signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1 signal in a manner identical to that described for Bit 0.

Bit 3 OUT 2 output, auxiliary user-designated output OUT2. Operation as OUT1.

Bit 4 Loopback when set to logic 1, normal operation when reset to logic 0. When set to logic 1 the following events occur:

a) the serial output is set to marking, logic 1
b) the serial input is disconnected
c) the output of the transmitter shift register is connected to the receive shift register
d) the following status bits are linked, CTS to DTR, DSR to RTS, RLSD to OUT1, RI to OUT2.

This enables all the 8250's functions and software to be checked. It should be noted that the interrupts are still operational.

Bits 5 to 7 There are no bits 5 to 7, they are all set to logic 0.

Modem Status Register (port x6/xE read/write)

Bit 0 Delta Clear To Send (CTS), if set to logic 1 indicates that the CTS line has changed state since the modem status register was last read.

Bit 1 Delta Data Set Ready (DSR), if set to logic 1 indicates that the DSR line has changed state since the modem status register was last read.

Bit 2 Trailing Edge Ring Indicator (RI), if logic 1 indicates that the /RI input to the 8250 has gone from logic 1 (high) to logic 0 (low) since the modem status register was last read. For further details on the ring indicator please refer to bit 6 of the modem status register.

Bit 3 Delta Received Line Signal Detector (RLSD), if logic 1 indicates that the RLSD has changed state since the modem status register was last read.

Bit 4 Clear To Send (CTS) input, logic 1 if the CTS input to G818 is positive, logic 0 if CTS is negative. If bit 4 (loopback) of the modem control register is a logic 1 this bit indicates the state of RTS (bit 1) in the modem control register.

Bit 5 Data Set Ready (DSR) input, logic 1 if the DSR input to G811 is positive, logic 0 if the DSR input is negative. If bit 4 (loopback) of the Modem Control register is logic 1, this bit indicates the state of DTR (bit 0) in the Modem Control register.

Bit 6 Ring Indicator (RI) input, logic 0 if the /RI input is high, logic 1 if the input is low. If bit 4 (loopback) of the modem control register is logic 1, this bit indicates the state of OUT 1 (bit 2) in the modem control register. It should be noted that on the GM818 the RI input is pulled up by a 10k resistor (R11/12) and it is also connected to pin 14/15 of link block 1 where it may be grounded. It is intended that this should be used by the software to indicate the board status.

Bit 7 Received Line Signal Detect (RLSD) input, logic 1 if the RLSD input to GM818 is positive, logic 0 if RLSD is negative. If bit 4 (loopback) of the modem control register is set, this bit indicates the state of OUT2 (bit 3) in the modem control register.

Interrupt Enable Register (port x1/x9 read/write)

Bit 7 of the line control register (port x3/xB) must be logic 0 for access.

Bit 0 Received Data Available Interrupt, when set to logic 1, an interrupt will be generated whenever data is available to be read.

Bit 1 Transmitter Holding Register Empty Interrupt, when set to logic 1, an interrupt will be generated whenever the Transmit Holding register becomes empty.

Bit 2 Receiver Line Status Interrupt, when set to logic 1, an interrupt will be generated whenever any of bits 1 through 4 of the line status register go high to indicate an error condition.

Bit 3 Modem Status Interrupt, when set to logic 1, an interrupt will be generated whenever any of bits 0 through 3 of the modem status register go high to indicate a change in modem status.

Bits 4 through 7 Always set to logic 0.

Interrupt Identification Register (port x2/xA read only)

Bit 0 Interrupt Pending, when logic 0 an interrupt is pending. When the interrupt identification register is accessed all interrupts are frozen and no further interrupts will be acknowledged until the cause of the interrupt has been serviced or cleared.

Bit 1 = logic 1 & bit 2 = logic 1

Highest level of interrupt priority, caused by a Receiver Line Status Register interrupt. Source of error, Overrun error, Parity error, Framing error or Break interrupt. Reset by reading the Line Status Register.

Bit 1 = logic 0 & bit 2 = logic 1

Second highest level of interrupt priority, caused by receive data becoming available. Reset by reading the Receiver Buffer register.

Bit 1 = logic 1 & bit 2 = logic 0.

Third highest level of interrupt priority, caused by the Transmitter Holding register becoming empty. Reset by either reading the Interrupt Identification register or by writing into the Transmitter Holding register.

Bit 1 = logic 0 & bit 2 = logic 0.

Fourth highest level of interupt priority, caused by a Modem Status register interrupt. Source of the interrupt is a change in status of one of the following signals, CTS, DSR, RI or RLSD. Reset by reading the Modem Status register.

Bits 3 thorugh 7 set permanently to logic 0.

Baud Rate Generator

Most significant byte, port x1/x9 read/write.
Least significant byte, port x0/x8 read/write.

Bit 7 of the Line Control Register (port x3/xB) must be set to 1 for access.

The baud rate is generated by dividing down the clock input of the 8250. The equation for determining the baud rate is as below:

$$\text{Divisor} = \frac{\text{8250 clock frequency}}{\text{(Baud rate x 16)}}$$

The divisor should be split into two bytes. The most significant byte should be loaded into the most significant Divisor Latch, the least significant byte being loaded into the least significant Divisor Latch. It should be noted that,

a) the divisor is in Hex
b) the bytes should be loaded even if zero (some 8250's have been observed to power up loaded with FF).

The divisors for a 2 MHz clock are tabulated below. The numbers in the hex column should be loaded.

Baud Rate	Divisor (decimal)	Divisor (hex) MSB	LSB
50	2500	09	C4
75	1667	06	83
110	1136	04	70
134.5	929	03	A1
150	833	03	41
300	417	01	A1
600	208	00	D0
1200	104	00	68
1800	69	00	45
2000	63	00	3F
2400	52	00	34
3600	35	00	23
4800	26	00	1A
7200	17	00	11
9600	13	00	0D

Data Holding Register (port x0/x8 write only)

Bit 7 of the Line Control register (port x3/xB) must be logic 0 for access. Data from this register is output from the 8250 in serial form.

Receiver Buffer Register (port x0/x8 read only)

Bit 7 of the Line Control register (port x3/xB) must be logic 0 for access. This register contains the received data.

Further data on the 8250 can be obtained from the relevant data sheet. (e.g. National Semiconductor INS 8250), or see 'An Introduction to Microprocessors Volume 3', by Osborne.

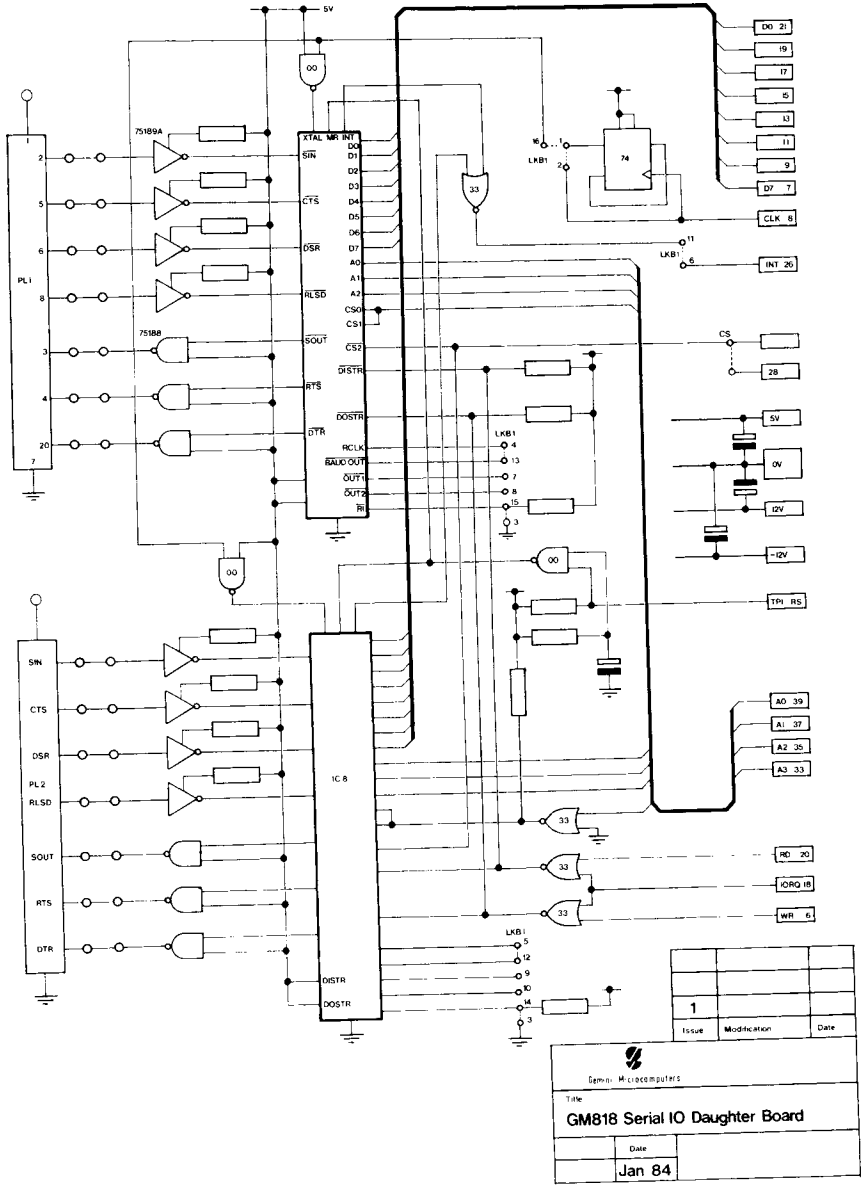
6. EXAMPLE SOFTWARE.

The following routines illustrate programming of the 8250 UARTs. The routines cover the initialisation of an 8250, status tests, and outputting and inputting of characters.

```
        .z80
;
; Example routines for supporting an 8250 UART
;

uart    equ     0a0H            ; UART base address

u$data  equ     uart            ; I/O data registers
u$lcr   equ     uart+3          ; Line control register
u$mcr   equ     uart+4          ; Modem control register
u$lsr   equ     uart+5          ; Line status register
u$dll   equ     uart            ; Divisor latch (low)
u$dlm   equ     uart+1          ; Divisor latch (high)

dvsr    equ     52              ; Divisor for Baud rate (2400 here)
umode   equ     0Fh             ; Mode word
uconf   equ     3               ; 8-bits, one stop bit, no parity

;*********************************
;       UART initialisation     *
;*********************************

init:   ld      a,umode         ; Set mode word
        out     (u$mcr),a
        ld      a,83H           ; Enter divisors
        out     (u$lcr),a       ; selects divisor latches
        ld      a, HIGH(baud)   ; Get Baud rate
        out     (u$dlm),a       ; Set it
        ld      a,LOW(baud)     ; Divisor low
        out     (u$dll),a
        ld      a,uconf         ; Set configuration
        out     (u$lcr),a
        ret

;*********************************
;       I/O routines            *
;*********************************
;
;  Serial status poll - Input
;  returns -
;       A=0     Not ready
;       A=FFH   Ready
;
sersti: in      a,(u$lsr)       ; Read status bits
        and     1               ; Check ready bit
        ret     z               ; Return Z if busy
        ld      a,0FFH          ; Ready - so FF
        ret
```

```
; Serial input - returns byte in A

serin:  in      a,(u$lsr)       ; Read status bits
        and     1               ; Check ready bit
        jr      z,serin         ; Loop if busy
        in      a,(u$data)      ; Ready, so read
        ret

;
;  Serial Handshake routine - Status check
;       Uses the CTS line on the 8250
;       If everything is Ok it falls through into the
;       the normal status poll routine

hsst:   in      a,(u$msr)       ; Read Modem control lines
        and     10H             ; Check the CTS line
        ret     z               ; Return if busy

;
;  Serial status poll - Output
;  returns -
;       A=0     Not ready
;       A=FFH   Ready
;
serst0: in      a,(u$lsr)       ; Read status bits
        and     20H             ; Check ready bit
        ret     z               ; Return Z if busy
        ld      a,0FFH          ; Ready - so FF
        ret

; Serial Output routine
;       Outputs the byte in C

serout: in      a,(u$lsr)       ; Read status bits
        and     20H             ; Check ready bit
        jr      z,serout        ; Loop if busy
        ld      a,c             ; get byte
        out     (u$data),a      ; Ready - so output byte
        ret

; List Output for handshaking printer
;       Outputs the character in C when ready

hshake: call    serst           ; wait until ready
        jr      z,hshake
        ld      a,c             ; Get the byte
        out     (u$data),a      ; Output it
        ret
```

7. CIRCUIT DIAGRAM



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