The Gemini MultiBoard Microsystem

Z80 IVC

80-BUS INTELLIGENT VIDEO CONTROLLER CARD

INSTRUCTION MANUAL AND FUNCTIONAL DESCRIPTION

G812
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Introduction

The G812 is an 80-BUS and Nasbus compatible video display card for use with Gemini Multiboard and Nascom systems. The design has been optimised to allow the major characteristics of the card (screen format, character set etc.) to be varied under software control. In its standard configuration it will display 25 lines of 80 characters. It can however be programmed to work in a large number of different configurations. All of the screen handling is taken care of by an on-board Z80A. Hardware features allow for the card output to be inverted or blanked under software control. Two dot clocks are provided for the video circuitry, one determined by a crystal and the other variable by adjusting a multi-turn potentiometer, RV1. The choice of clock is under software control. The character set of the card may be held in EPROM or RAM. The normal configuration is to have 128 characters fixed in EPROM and 128 characters held in RAM, and consequently alterable under software control. A keyboard port and light pen socket are also provided. The interface to the host system is via three I/O ports.

This manual is in two sections, a user section instructing the user in commissioning the G812 and a functional description section detailing the design. The on-board monitor program controlling the G812 Intelligent Video Controller (IVC) card is described in a separate software manual.

Contents

Commissioning

Carefully unpack your G812 and examine it for any mechanical damage. In the event of any damage please inform your dealer immediately.

Your G812 will have been shipped to you fully tested and working. All that may be required is for the board to be plugged in. However, please take the time to read through this manual as it will prove useful.

When plugging the G812 into the bus please take great care. Excessive force should not be required. Any difficulty that may be encounted will, in all probability, be due to the keyway of the edge connector not fitting accurately into the slot in the edge of the card. Please ensure that the card is plugged in with the edge connector going in first and the correct way around. It is not possible to plug the board in the incorrect way around because of the keyway.

There are six linking options on the G812. The standard link positions will have been set during manufacture. However, full details are provided in the section on links to allow the user to configure the card for his own requirements.

Connectors

There are three I/O connectors on the G812 (Video, Keyboard and Light pen). The connections are detailed below.

a) Video Connector

The video connector is a 1/4 inch jack plug, the tip carrying the video signal and the sleeving acting as the ground. The monitor to be used should be connected via low-loss coaxial cable. If low-loss cable is not used the picture quality may be poor.

b) Keyboard Connector

+5 volts	1	2	Strobe
Ground	3	4	Ground
D5	5	6	D4
D6	7	8	Ground
Ground	9	10	D2
D3	11	12	D0
D1	13	14	Power Led drive
-12 volts	15	16	No connection

The keyboard port is for a standard ASCII keyboard with a positive strobe i.e. Gemini G613. Care should be taken to ensure that the keyboard is connected the correct way round, otherwise it may be damaged.

c) Light Pen Connector

Ground	2		
+5 volts	4	5	Strobe
+12 volts	1	3	Enable

The connector is the standard five pin DIN connector. For full details please see the manual provided with the light pen. (Connector viewed from front).

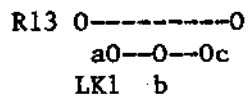
Adjustable Dot Clock.

G812 is provided with two sources for the dot clock used in the video circuitry. One is controlled by a crystal (XTAL - normally 16 MHz), and the

Links

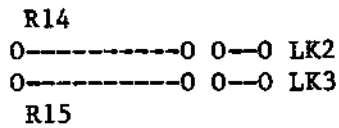
There are six linking options on the G812. The standard link positions will have been set during manufacture. However, full details are provided below to allow the user to configure the card for his own requirements. All links should be made by soldering wire from one connection to the other. Please take great care as an incorrect link may cause damage and a poor connection will result in an unreliable system.

Link One. (LK1). 2716 or 2732 EPROM selection.



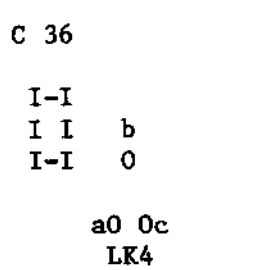
This link is used to select the type of monitor EPROM (IC 18 - IVC-MON) which is to be used. For a 2716 link 'b' to 'c', for a 2732 link 'b' to 'a'. A 2716 is standard but a 2732 software enhancement may become available.

Links Two & Three. (LK2 & LK3). USR 1 and 2.



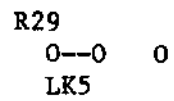
The state of these links can be read by the IVC-MON program to determine power-on default conditions, so for full details please see the software manual. They do not have any effect on the hardware.

Link Four. (LK4). Sync selection.



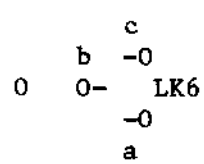
Link four determines whether the vertical or horizontal sync signals are linked to the Z80's /NMI input. This facility informs the software when it is in a blanking period. This link will normally be from 'a' to 'b'.

Link Five. (LK5). /NASIO provision.



Link five determines whether or not the G812 generates a /NASIO signal onto the bus. If the link is made a /NASIO signal will be generated. The /NASIO is only required for Nascom 1 and 2. Only one board in a system should generate /NASIO. The G811 does not require it. If used with a Nascom then the IOEXT link (Nascom 1) or switch (Nascom 2) should be set to 'External'. With Nascom 1 there is a decode fault that necessitates the removal of the Z80 PIO when external I/O is used.

Link Six. (LK6). Clock selection.



Link six determines the source of the Z80 clock on the G812. If 'b' is linked to 'a' the clock will come from the AUX CLK line. If 'b' is linked to 'c', the clock will come from the main system clock line, and this is the normal condition. The G812's Z80 has to run at 4MHz for correct operation. If the host system is running at 4MHz the G812's Z80 can be clocked with the same signal. However, if the G812 is to be used with a 2MHz system a 4MHz clock should be provided on the AUX CLK bus line and 'b' should be linked to 'a'. For full details on implementing the AUX CLK line please see the manual for the bus master.

G812 FUNCTIONAL DESCRIPTION

Contents

Section 1 - Processor Circuitry

1.0 Z80 clock

The clock for the Z80 can come from one of two sources. In a 4MHz system the Z80's clock would come from the system clock line (Gemini 80-BUS line 5). However if the G812 is to be used in a system which does not run at 4MHz, a 4MHz signal should be provided on line 8 of the bus (AUX CLK), the choice of clock signal being determined by link 6. The clock signal is buffered by a 74LS04 (IC 29b) the output of the LS04 being used to clock the 74LS74 flip-flop (IC 31b) (see section 3.0 for further details). The clock is further inverted by a second 74LS04 (IC 29c) which drives the Z80 clock driver circuitry. The Z80 clock driver is a push pull circuit formed by transistors TR2 and TR3.

1.1 Z80 reset

The reset signal to the Z80 can come from one of two sources. On power-up C44 (47uF) will be discharged and consequently the reset input to the Z80 will be held low via the 1N4148 diode D1 and this will cause the Z80 to reset. The capacitor (C44) will charge up via Rs 28 (47k), 24 (220R) and the diode D1. Diode D1 is present to ensure that once the capacitor (C44) is charged its presence will have no effect on the reset from the host system. When the G812 is powered down, C44 is discharged via the diode D2 (1N4148). If this is not done the G812 may fail to reset due to C44 remaining charged.

The second source of reset is by the host system accessing port B3 (in the standard configuration which could be changed). An access of port B3 would be detected by the bipolar PROM (IC 35)(see section 2.1), the output of the PROM being connected to the Z80 via a 220R resistor R24. When the PROM detects an access of port B3 its D3 output will go low for the duration of the host systems I/O cycle causing the reset input to the Z80 to go low.

1.2 Z80 control signals

Apart from the clock and the reset input only five of the Z80's control signals are implemented. /RD is used as the read signal, /WR is used as the write signal, /IORQ is used to enable the CRTC and /MREQ is used to enable everything else. /NMI can be connected either to the H sync or to the V sync outputs of the CRTC by the appropriate setting of link 4. This enables the software to determine the video timing. /M1, /HALT, /RFSH, and /BUSAK are not connected. /BUSRQ, /WAIT and /INT are all pulled high by the 2k2 resistor R18.

1.3 Z80 I/O and memory decoding

The Z80 memory space is decoded into eight blocks of 8K bytes with the following assignments;

Address	Function
0000 - 1FFF	Z80 program EPROM
2000 - 3FFF	VDU RAM
4000 - 5FFF	Character generator memory
6000 - 7FFF	G812 status port (read only)
8000 - 9FFF	Keyboard port
A000 - BFFF	Data port
C000 - DFFF	G812 status port (write only)
E000 - FFFF	Z80 RAM area

The decoding is done by a 74LS138 (IC 26), the LS138 being a one of eight decoder. A13, 14 and 15 are input along with /MREQ which is used to enable the LS138. The I/O ports are not decoded as /IORQ is only used to enable the CRTC.

1.4 Z80 memory

The Z80 has two memory sockets for its use, an EPROM socket for the Z80's program and a 2K RAM socket. The /CE of the program EPROM (IC 18) is connected to the LS138 decoder. /RD is input to the /OE (output enable) input of the EPROM to prevent a data bus clash in the event of a write to the EPROM. The EPROM socket itself can, with the appropriate setting of link 1, be used for either a 2716 or a 2732 type EPROM. In the 2716 setting the link applies +5 volts via a 220R resistor R12 to the Vpp input (pin 21). In the 2732 setting A11 is connected to pin 21.

1.5 G812 status port

The status port is in two sections, a read section and the write section. The read section is decoded at address 6000H. The bit assignments are as detailed below.

Bit	Function
0	Data transfer handshake in
1	Vertical sync status
2	Horizontal sync status
3	Display enable status
4	Light pen strobe
5	Link 2 status
6	Link 3 status
7	Data transfer handshake out

Bit 0, data transfer handshake in, this bit is set by a write (of data) from the host and reset by a read of the data by the G812.
Bit 1, vertical synchronisation pulse output from the CRTC, this bit is high during the vertical sync pulse period.
Bit 2, horizontal synchronisation pulse ouput from the CRTC, this bit is high during the horizontal sync pulse period.
Bit 3, display enable output of the CRTC, this bit will be low when the display is disabled.
Bit 4, light pen strobe input to G812, would normally go high to indicate that the switch on the light pen had been activated.
Bit 5, link 2, if link 2 has been made (connected) this bit will be low.
Bit 6, link 3, if link 3 has been made this bit will be low.
Bit 7, data transfer handshake out, set by a read of data by the host, reset by a write of data by the G812.

The second half of the G812 status port is the write (at C000H) section. The bit assignments are as detailed below.

Bit	Function
0	Display disable
1	Dot clock select
2	Invert the entire screen area
3	CRTC reset
4 to 7	Unused

Bit 0, if taken low the display will be disabled.
Bit 1, low to select the adjustable dot clock, high to select the crystal dot clock.
Bit 2, low for normal video, high for inverse video.
Bit 3, reset input to the CRTC, if taken low then high the CRTC will reset.

Section 2 - IVC-Host Interface

2.1 Host system port decoding

The G812 occupies three I/O ports belonging to the host system. The first port is for the transfer of data between the host and the G812. The second port is for the handshake signals between the host and the G812. The third port is to enable the host system to reset the G812 as the bus reset line is not connected to the G812. The bottom eight address lines are connected to the eight address inputs of the port decode PROM (IC 35). /IORQ is connected to the /CE input of the PROM to ensure that it only decodes valid port addresses.

Three data outputs from the PROM (D0, D1 and D2) are pulled up by the 2k2 resistors (Rs 25, 26, and 30) and the fourth output (D3) is pulled up with a 47k resistor (R 28), this being done to ensure that the outputs remain high when the PROM is not enabled. The data outputs from the PROM are assigned as detailed below.

Data output	Function
D0	/NASIO
D1	Data transfer
D2	Handshaking
D3	Reset

The PROM is coded in the following manner.

a) Select the ports to which you wish the above functions to be assigned. It would be usual to assign the lowest eight ports to decode a Nascom 1 or 2 via /NASIO. Note that the G811 does not require any external decoding.

b) The 256 locations in the PROM are directly mapped to the 256 I/O ports available. One merely has to load the particular location in the PROM with the contents which will take the appropriate data output low and enable the specific circuitry.

c) D0 will go low if the location contains an E, D1 will go low if the location contains a D, D2 will go low if the location contains a B and D3 will go low if the location contains a 7.

Below is a table of contents for the standard G812 PROM. (VID-1).

PROM location	Contents	Function
00 - 07	E	/NASIO
08 - B0	F	No function
B1	D	Data port
B2	B	Handshake
B3	7	Reset
B4 - FF	F	No function

For a full list of PROM part numbers see section 4.0.

2.2 /NASIO decode

The D0 output of the PROM is used to generate the /NASIO signal which enables the onboard ports on a Nascom 1 or 2 (the ports not being fully decoded). The /NASIO signal is a pseudo open collector signal that is generated in the following manner. The D0 ouput of the PROM will go low to indicate that a port

2.3 Data transfer

The D1 output from the I/O decode PROM is used to enable the host side of the data transfer circuitry. The data transfer is effected with the use of two 74LS374's (IC's 27 and 32). The LS374 is a an octal D-type flip-flop with tristate outputs. It has two control signals, a clock input which strobes the data into the device on the low to high edge and an output enable input which when taken low enables the outputs. One LS374 (IC 32) is configured to transfer data from the G812 to the host system. The data is strobed into IC 32 by a signal from the 74LS32 (IC 34b). The LS32 ORs together the signal from the LS138 (which decodes the memory addresses) (see section 1.3) with the write signal from the Z80. The outputs from IC 32 are enabled by the D1 output from the PROM ORed with the read signal from the bus by the 74LS32 (IC 34a). This ensures that the outputs are only enabled by a read of the appropriate port (B1).

The second LS374 (IC 27) is connected in a similar manner but configured to latch data from the host system and transfer it to the G812. Data is clocked into IC 27 by the low to high of the signal created by the 74LS32 (IC 34d) which OR's together the D1 output of the PROM with the write signal from the host system. The outputs of IC 27 are enabled by the signal from the 74LS32 (IC 34c) which OR's together the output of the LS138 decoder (IC 26) with the read signal from the G812's Z80.

2.4 Handshaking

Handshaking signals are provided to speed up the transfer of data between the G812 and the host. The handshaking lines operate in the following manner. The handshaking line (D0) for data into the G812 will go high when data is strobed into the LS374 (IC 27) by the host. When the G812 reads the contents of the LS374 (IC 27) the handshaking line will go low. For data out of the G812 to the host system the handshake line (D7) will go high when data is written by the G812. When the host reads the data, the handshake line will be taken low.

The hardware consists of an RS flip-flop for each handshake signal. The flip-flop for data into the G812 consists of the two 74LS00 NAND gates (IC33 c/d). The set input of the of the flip-flop is connected to the clock input of IC 27. The reset input is connected to the output enable input of IC 27. The output of the flip-flop is connected to two places, the 74LS125 tristate buffer (Ic 28d) and the status port formed by the 74LS244 (IC 19) (for further details see section 1.5). The LS125 is enabled by the D2 output of the I/O decode PROM (see section 2.1) ORed with the read signal from the host system by the 74LS32 (IC 30a). The output of the LS125 is connected to the D0 data line of the host system.

The RS flip-flop associated with the transfer of data from the G812 to the

2.5 /DBDR generation

For full compatibility with Nascom 1 and the Supermum the G812 has to generate a /DBDR signal. /DBDR has to be taken low whenever the G812 outputs data to the bus. The G812 can output data either from the data transfer port (IC 32) or from the handshake port (IC 28a/d). The 74LS08 (IC 3d) has one input connected to the /OE of the LS 374 (IC32) and one input connected to the enable signal of the LS125s (IC 28a/d). Whenever either signal is taken low, the output of the LS08 will go low. The output of the LS08 enables the LS125 (IC 28b) to take /DBDR low.

Section 3 - Video Circuitry

3.0 CRTC implementation

The HD46505S is a CRT controller (CRTC). It is clocked by the character rate clock (from which all the timing is derived) and from that it will generate all the necessary addresses and synchronisation pulses. Before detailing the implementation of the CRTC some of its background has to be explained to avoid any confusion. Originally there was an IC known as the 6845R. The 6845R was redesigned and became known as the 46505S. The 46505S has since also become known (and available) as the 6845S. A third IC (the 6545) is also similar. There are small, but very significant, differences between the three ICs, extending from the hardware implementation to the software programming. If it is intended to reprogram the CRTC please ensure that you have the correct information, as programming the 46505S/6845S as though it was a 6845R (or 6545) will in all probability cause peculiar things to happen. All references to `CRTC' in this document refer to the 46505S/6845S.

Hardware implementation

The CRTC can be divided into two sections, the section which interfaces to the Z80 and the section which interfaces to the video circuitry.

The Z80 interface consists of the usual eight bidirectional data lines, a reset input, read/write input, a strobe input, register select input and a chip enable. The reset input is connected to bit 3 of the write side of the control port (see section 1.5). To reset the CRTC this bit should be taken low then high again. The CRTC will only reset if the light pen strobe input is low. All outputs will go low when the reset input is taken low and all the counters are cleared but not the registers. When the reset input is taken high the CRTC will immediately restart. The read/write input is connected to the Z80 write line, this input being taken low to write data to the CRTC. The CRTC is a 6800 family IC and as a consequence it requires the provision of a low to high strobe on the E input to input or output data. This is accomplished with the use of a 74LS74 D-type flip-flop (IC 31b). The flip-flop is clocked with the CPU clock and has its D input connected to the CRTC's /CE line. The /Q output of the flip-flop is connected to the E input of the CRTC. With the CRTC not selected the E input will remain low. When the /CE input to the CRTC goes low, the E input will remain low until the next low to high of the clock at which point the E input to the CRTC will go low to high to strobe the data in or out. The register select input switches between the two ports available to the Z80. It is connected to A0 which results in the address register being port 0 and all the other registers being port 1. The chip enable is connected to the Z80's /IORQ line.

The video section of the interface consists of the VDU RAM address lines, the character row select lines, the cursor enable output, the light pen strobe input and the two synchronisation (horizontal and vertical) signals. The eleven VDU RAM address lines (A0 to A10) are connected to the three 74LS157 multiplexers (ICs 10, 11 and 12) which switch the address lines for the VDU RAM between the CRTC and the Z80. The four character row select lines are connected to the 74LS157 multiplexer (IC 17) which switches the lower four address lines of the character generator between the CRTC and the Z80. The cursor output is connected to the 74LS86 EXOR gate (IC 2d). When the CRTC reaches the address of the cursor character the cursor output will go high and as a consequence the serial video data will be inverted. The display enable output enables the display by going high whenever information is to be displayed on the screen. The display enable signal is connected to the 74LS08 (IC 3c) where it is ANDed with the display enable signal from the status port (please refer to section 1.5). The output of IC 3c is connected to the 74LS08 (IC 3a) which AND's the serial video data with the display enable signals. The light pen strobe input is pulled low with the 47k resistor R10. This is necessary because the CRTC will not reset if the light pen strobe input is high. The last two signals are the horizontal and vertical synchronisation signals. These are EXORed together by the 74LS86 (IC 2a) and the output of IC 2a is inverted by the 74LS04 (IC 5f).

CRTC software

Access to the registers in the CRTC is obtained by loading the address register (port 0) with the address of the register that is of interest. All the other registers are accessed via port 1 so the method of register access is to output to port 0 the number of the register and via port 1 input or output operations can be performed.

Register 0, Horizontal total register (write only)
The number loaded into this register determines the line scan frequency of operation.

$$N = \left(\frac{\text{Line period}}{\text{Character period}} \right) - 1$$

The line period for a European type system would be 64u seconds and for an American system 60u seconds. The character period will vary with different dot clock frequencies (it is the dot period multiplied by eight). If it is proposed to run in the interlaced mode the number loaded must be odd.

Register 1, Horizontal displayed (write only)
This register is loaded with the number of characters that are to be displayed. It is usual practice for the displayed line to be 40u seconds long (the 64u seconds of a European type system being divided into 52u seconds of

Register 3, Sync width (write only)
The top four bits determine the width of the vertical sync pulse. The vertical sync pulse width is programmed in units of scan lines. If a 64u second line is being used, the width of the vertical sync pulse is programmed in units of 64u seconds. The number of scan line units is directly programmed into the top four bits with the exception of 16 scan lines which is programmed by loading the top four bits with 0. The broadcast T.V. specification calls for 2 1/2 lines of vertical sync. The 6845R (old version) was fixed at 16 lines. 16 lines should be used unless it gives problems, i.e. load with 0.

The horizontal sync pulse width is programmed in units of character period. The period of the desired sync pulse is divided by the character period to obtain the number for the lower four bits. Unlike the vertical sync register the horizontal sync width register cannot be loaded with 0. The broadcast T.V. specification calls for 4.7u seconds (European and American).

Register 4, Vertical total (write only)
The value loaded into this register is the total number of character rows (including the vertical retrace period) per frame - 1. i.e. if the total number of character rows per frame was to be 26 this register would be loaded with 26-1 (19H). It should be noted that this register is only a 7 bit register. One character row period is equal to the number of lines per character multiplied by the line period.

Register 5, Vertical total adjust (write only)
This register is programmed in units of scan lines to adjust the frame frequency to match the mains frequency. If the frame frequency is not the same as the mains frequency the picture will "wobble".

Register 6, Vertical displayed (write only)
This register is programmed with the number of character rows that are to be displayed. If, for example, 25 lines were to be displayed this register would be loaded with 19H (25).

Register 7, Vertical sync position (write only)
This register is programmed in units of horizontal character line period-1. If the position of the sync pulse is to be row 26, the register would be loaded with 26-1 (19H).

Register 8, Interlace and skew register (write only)
This register programs the video format and the skew factor. The appropriate value for loading into the register is obtained by adding up the values pertaining to the desired characteristics in the table below.

Video mode	
Non interlace	00
Sync interlace	01
Sync + video interlace	03
G812 skew factor	A0

The choice of interlace mode is determined by whether the same dot information is displayed in both fields or whether different information is displayed in the two fields (Sync + Video interlace). It is not recommended that interlaced video be used unless a long persistence monitor is also to be used. This is because interlaced video gives rise to a 25 Hz vertical jitter that can be very fatiguing. The skew factor is set by the hardware design of the G812. For non interlaced operation load the register with A0, i.e. A0 for the skew factor + 00 for the video mode.

Register 9, Scan lines per character (write only)
This register is loaded with the number of lines per character-1 for the non-interlace and sync interlace modes. For the video and sync interlace mode the register is loaded with the number of lines-2. This register programs the counter which controls the four row select lines which are connected to the lower four address lines of the character generator.

Register 10, Cursor start and display register (write only)
The lower five bits of this register are used to program on which line of the character the cursor display starts. The cursor display inverts the video information when it is enabled. Bit 5 and 6 determine the format of the cursor. The table below details the options.

Option	Bit 6	Bit 5
No blink (on all the time)	0	0
Cursor disabled	0	1
Blink (16 field cycle)	1	0
Blink (32 field cycle)	1	1

Register 11, end of cursor (write only)
The contents of this register determine on which line of the character that the cursor display ends.

Registers 12 and 13, start address register (read/write)
These two registers determine the VDU memory address at which the display starts. Register 13 holds the least significant part of the address and register 12 holds the most significant part of the address.

Registers 14 and 15, cursor location (read/write)
These two registers determine the actual location of the cursor in the display. Register 15 holds the least significant part of the address and register 14 holds the most significant part of the address.

Registers 16 and 17, light pen address register (read only)
These registers are used to catch the address of the light pen. Register 16 holds the most significant part of the address and register 17 holds the least significant part of the address. For further details on the light pen please refer to section 3.6.

Point to note. The CRTC registers should only be changed during the blanking period. If the registers are changed during display a flicker will be observed.

3.1 VDU RAM

The VDU RAM (IC 9) is a 2K X 8 static RAM chip of the "Bytewide" variety. Type numbers include 2016, 4016 and 6116 the latter being a CMOS chip. The eleven address lines (A0 to A10) can be connected either to the CRTC or to the Z80 the selection being performed by three 74LS157 multiplexers (IC10, 11 and 12). The LS157 (IC 12) is also used to switch the /OE input of the VDU RAM between /RD and ground (CRTC). The Z80 has priority over CRTC for the VDU RAM. When a VDU address is detected by the 74LS138 decoder the select inputs of the LS157s are taken low to switch the address lines from the CRTC to the Z80. The write line from the Z80 is ORed with the VDU RAM select signal by the 74LS32 (IC 6a), the net result being that if the VDU RAM is selected and /WR is low the write enable input to the VDU RAM will go low. The /CE input of the VDU RAM is permanently grounded.

The eight data lines from the VDU RAM are connected to a 74LS245 (IC8) which connects the Z80's data bus to the VDU RAM. The enable input of the LS245 is connected to the VDU RAM select signal and the direction input is connected to the Z80's read signal. The data lines are also connected to a 74LS273 eight bit latch (IC 14). The latch is used to latch the data out of the VDU RAM and hold it stable for the character generator. Data is latched by the same signal which loads the PISO.

3.2 Character generator

The character generator translates the character codes into dot patterns which are displayed. Any one of 256 characters is possible. The least significant 128 characters are translated by IC 20 and the most significant 128 characters are translated by IC 24. In the standard configuration the lower 128 characters would be the standard ASCII character set plus "standard" graphics and the higher 128 characters would be programmable characters for graphics use. To the G812's Z80 the character generator will appear as a 4K block at 4000H. Normally the lower 2K will be an EPROM and the upper 2K will be RAM. However both ICs could be EPROMs or both could be RAMs. To generate a character the eight bits from the VDU RAM together with four bits from the CRTC generate a 12 bit address which accesses a specific byte in one of the memory chips. The eight bits are then formed into a serial bit stream by the 74LS165 PISO (IC 23), the most significant bit going out first (so it will be on the left hand side). The eight bits from the VDU RAM are the actual character and the four bits from the CRTC are the actual line in that particular character. Three 74LS157's (ICs 15, 16 & 17) are used to switch the address lines of the character generator between the Z80 address lines and the VDU RAM + CRTC. The character generator data lines are buffered by a 74LS245 (IC 22). /RD is used to control the direction and the buffer is enabled by the same signal that is used to enable the character generator.

3.3 Video timing and dot clock

The video timing is all derived from the dot clock generator, the dot clock generator being a 74LS629 (IC 7) which is a dual voltage controlled oscillator. Half of the LS629 (IC 7b) is configured as a crystal oscillator. The other half is a voltage controlled oscillator whose frequency of oscillation is controlled by the ten turn 10k potentiometer RV1. Adjusting RV1, will vary the frequency of oscillation and hence the dot clock frequency. The range of the LS629 oscillator is set by the two resistors R12 and R11. The frequency of oscillation may also be changed by varying the 12pF timing capacitor (C14). The actual dot clock frequency can be measured at the two pins provided on the edge of the board. The choice of dot clock is determined by bit 1 of the write status port. If low, the variable dot clock is selected, if high, the crystal dot clock is selected. Bit 1 is connected directly to the enable input of the variable dot clock and to the enable input of the crystal dot clock via a 74LS04 inverter (IC 5d). The output of the disabled oscillator will be high. The two outputs are ANDed together by the 74LS08 (IC 3b).

The dot clock is connected to a 74LS93 binary divider which divides the dot clock by eight to generate the character clock. The character clock is resychronised to the dot clock by the 74LS74 (IC 31b). The load pulse for the 74LS165 PISO is generated by the 74LS32 (IC 30b) which OR's the Q output of the LS 74 with the /Q output delayed by the two 74LS04 inverters (ICs 29a and d). This gives a 20nS pulse for loading the LS165 and the LS273 latch (IC 14). The clock input to the LS165 is via the two 74LS04 inverters (IC 29c and f) which bring the clock back into time with the load pulse.

3.4 Video interface circuitry

The serial data output from the 74LS165 (IC 23) is connected to the 74LS86 (IC 2d) EXOR gate. The other input to the EXOR gate is connected to the cursor enable output of the CRTC. The EXOR gate will invert the serial data whenever the cursor output of the CRTC is high.

The output of the 74LS86 (IC 2d) is connected to the input of a second LS86 (IC 2c). The other input to the LS86 is connected to the write status port. This makes it possible to invert the entire picture. If bit 2 of the status port is high the picture will be inverted, if it is low the picture will not be inverted. The output of the LS86 is connected via the 74LS32 OR gate which is used to stabilise the timings to the 74LS08 AND gate (IC 3a).

The display enable output of the CRTC is ANDed with the display enable signal from the status (write) port (Bit 0) by the 74LS08 (IC 3c). If either of the signals is taken low the display will be be blanked. The output of IC 3c is connected to IC 3a.

Both the synchronisation (horizontal and vertical) outputs from the CRTC are active high, i.e. they will go high to generate a synchronisation pulse. Both outputs are EXORed together by the 74LS86 (IC 2a). This is done to ensure that line sync is available during the frame flyback. The output of the LS86 is inverted by the 74LS04 (IC 5f).

The synchronization pulses and the video data are mixed at the base of the 2N3904 transistor TR1. The 3904 forms a common emitter output stage. The output impedance is defined by the 68 ohm resistor R7. The output is A.C. coupled with the 100uF capacitor C7 with a 100nF "peaking" capacitor in parallel to improve response at high frequencies.

3.5 Light pen

Provision has been made for a light pen. The connection is via a 5 pin DIN connector which provides +12 volts +5 volts and ground. The light pen connector has two inputs, a strobe input which is a "cleaned up" version of the phototransistor output and a switch input which indicates the state of the switch on the light pen. The light pen input to the CRTC is pulled low with a 47k resistor to ensure that when no light pen is connected the input is low. The CRTC will not reset when the light pen strobe input is high. The CRTC will latch the character address when the light pen input goes low to high. However the CRTC only checks the light pen input when the character clock goes high to low. The address in the light pen registers is the address which the high to low transition caused.

3.6 Keyboard port

Section 4 - PROM types

The PROM is a 256 X 4 open collector type. The part is available from numerous sources, programming however is unique to each part. For a custom PROM please contact Gemini or your Gemini distributor.

Brand	Part number
AMD	27S20C
Fairchild	93417DC
Fujitsu	MB7052
Harris	7610-5
Intel	3621
Intersil	5603AC
MMI	6300-1
Nat semi	74S387
NEC	uPB403D
Signetics	N82S126
Texas	74S387 - recommended part