



# Gemini Microcomputers

Oakfield Corner Sycamore Road Amersham Bucks HP6 5EQ  
Telephone (02403) 22307 Telex 837788

~~NASBUS COMPATIBLE EPROM/ROM CARD~~

Construction and Functional Specification Documentation

## Introduction

The Gemini Microcomputers EPROM card has been designed to accommodate sixteen 2708 (1k x 8) or 2716 (2k x 8) type memories. Also included on the card is a socket for the Nascom 8k Basic, 36000 series ROM. The cards memory section is organised in four Banks of four sockets. Each Bank may contain up to four 2716s or four 2708 EPROMS. The mixing of 1 and 2k EPROMS in one Bank is not permitted. Each of the four Banks and the 8k EPROM may be decoded to start at any Z80 4k address boundary. A wait state generator is included, which can be activated only when the card is being accessed. This feature allows any dynamic memory in the system to run at 4Mhz without wait states, thus effecting faster program execution time.

This card also supports the Nascom Page Mode facility which allows up to 4 Nascom RAM B or EPROM/ROM cards to be used within the system. This facility allows the EPROM card to be brought into the system address space only when it is required. The page at which this card will reside is selected by four DIL switches. Address selection is accomplished by means of links on a 24 pin header plug. Two other pins on the header plug allow control of Nascom 1 M.EXT signal and wait state disable.

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## Component list

No.	Qty.	Description	Circuit. Ref.	Check
<b>INTEGRATED CIRCUITS</b>				
01	3	<del>81LS95</del> Octal Tri-state Buffer	ic 1, 2 & 3	( ✓ )
02	2	74LS156 O/c Dual 2 to 4 line Decoder	ic 4 & 5	( ✓ )
03	1	7406 O/c Hex Inverter	ic 6	( ✓ )
04	1	74LS04 Hex Inverter	ic 7	( ✓ )
05	1	74LS132 Quad 2 input OR gate	ic 8	( ✓ )
06	2	74LS139 Dual 2 to 4 Decoder	ic 9 & 10	( ✓ )
07	1	74LS20 Dual 4 input Nand gate	ic 11	( ✓ )
08	1	74LS74 Dual D-type Flip-flop	ic 12	( ✓ )
09	1	74LS00 Quad 2 input Nand gate	ic 30	( ✓ )
10	1	74LS30 Eight input Nand gate	ic 31	( ✓ )
11	1	74LS175 Quad D-type Flip-flop	ic 32	( ✓ )
<b>RESISTORS</b>				
12	5	4k7 .25w 10% Hystab Yel-Nau-Red	R1to4/13	( ✓ )
13	7	2k2 .25w 10% Hystab Red-Red-Red	R5 to 11	( ✓ )
14	1	220R .25w 10% Hystab Red-Red-Brn	R14	( ✓ )
15	1	1k .25w 10% Hystab Brn-Blk-Red	R15	( ✓ )
<b>CAPACITORS</b>				
16	3	10Mfd 16v Tantalum Bead	DC1 to 3	( ✓ )
17	55	10n 20v Ceramic disc	Decouple	( ✓ )
<b>IC SOCKETS</b>				
18	18	24pin .6in DIL		( ✓ )
19	3	20pin .3in DIL		( ✓ )
20	5	16pin .3in DIL		( ✓ )
21	7	14pin .3in DIL		( ✓ )
<b>MISCELLANEOUS</b>				
22	1	Green .2in diam. LED	LED 1	( ✓ )
23	1	<del>BC108</del> (or equiv) Transistor	TR 1	( ✓ )
24	1	ERG 4xSPST DIL switch	SW1-4	( ✓ )
25	12	4 pin Stripline plugs		( ✓ )
26	1	NASBUS 78 way edge connector	PL1	( ✓ )
27	1	G803 D/S, PTH PCB 8in x 8in		( ✓ )
28	1	24PIN DIL PLUG		( ✓ )

Please check off components using ( ) boxes.

6 LINKS

887 SOLDERED JOINTS

## Construction hints

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1. Do not begin construction now. Read through all the documentation at least twice before starting in order to ensure that no fundamental and expensive errors are made.
2. When handling EPROMS and ROMS, observe MOS handling instructions as outlined in the Nascom 1 and 2 manuals.
3. Keep the box in which the EPROM card was delivered in case it should have to be returned for repair.
4. Do not attempt to use too large a soldering iron. Use an earthed 15 to 25 watt soldering iron equipped with a suitably small bit. Use 22 Swg resin-cored solder.
5. Fit all components in the board on the same side as the printed information.
6. Be certain to fit all integrated circuits and tantalum bead capacitors in the correct locations and the correct way round.
7. Be certain to connect the power supplies to the Bus the correct way round. (See Nasbus functional specification).
8. Do not attempt to remove or plug in integrated circuits on the board, or perform any soldering while the power supply is switched on.
9. If any difficulty is experienced when plugging an IC into its socket do not use extreme force. If in doubt remove the IC; check that the pins are straight and parallel and start again. An IC insertion tool may be found useful. Note that all ICs are manufactured with the leads spread apart by a few degrees to suit mechanised handling equipment. They can be bent parallel with care using small pliers or one row at a time by pressing down sideways on a flat surface. There should be no bend in the leads and they should be at right angles to the body.
10. Before switching on any power supplies, hold the board up against a powerful lamp and inspect both sides with a magnifying glass for solder splashes, unsoldered joints, incorrectly orientated components and bent IC pins. (To check for the latter look at all ICs end on). TAKE TIME OVER THIS.
11. The following tools are needed:-
  - (a) Long nose pliers
  - (b) A powerful light source
  - (c) A multimeter - not necessary, but useful to check supplies
  - (d) Side cutters
  - (e) A magnifying glass - for inspecting the PCB
  - (f) 15 to 25 watt soldering iron
  - (g) A damp sponge or cloth - to keep iron bit clean

### Suggested order of construction

1. Unpack the kit and check the components against the Parts List. Inspect the printed circuit board (PCB) for any signs of damage or manufacturing faults.
2. IC SOCKETS Check to see that all IC sockets do not have their pins bent or missing. During insertion take care not to bend any pins. When soldering the IC sockets, it may be a good idea to solder only two pins, one at each end of the socket on opposite rows to begin with. Then turn the board over again and check that the sockets are flat on the board, straight and also correctly orientated. See Fig.1 for typical socket orientation markings. Any necessary alterations may be carried out with ease, as only two pins have been soldered.
3. RESISTORS Preform the leads at rightangles to the resistor body so that they comfortably fit in the resistor pads as marked on the board. The resistors may be held in place after insertion by bending the leads about 40 degrees outwards. Solder the resistors.
4. CAPACITORS Insert and solder (1) the 55 10n ceramic capacitors and (2) the 3 tantalum capacitors. These tantalum capacitors are electrolytic and, as such, must be correctly orientated. See Fig. 2 for orientation markings.
5. Solder in place TR.1. The emitter of this transistor is identified by a tab on its can near this pin.
6. LED Preform the LED wires to fit in the LED pads. The + side of the LED can be identified by a shorter wire.
7. LINKS Link 1 need only be inserted if (A) Page Mode is used and (B) no other card in the system is providing an I/O EXT signal (i.e. Nascom I/O card). For normal Page Mode operation, insert a link in LK6. If Page Mode is not used, SW 1 to 4 need not be used and a link should be inserted in LK5. LK2, 3 and 4 are intended to be used for extended Page Mode operation.
8. INTEGRATED CIRCUITS Insert the ICs as outlined in the Components List on page 1-2. When completed, check that all ICs are correctly orientated and in the right position.
9. Take a final look at the card and check that there are no unsoldered pins or solder bridges anywhere.
10. When satisfied everything is correct, plug the board into the system. Power up the system and, if a multimeter is available, check the supply voltages. Check Nascom 1 or 2 for normal operation. Turn to page 2-2 for address decoding and EPROM selection information.

Fig. 1a

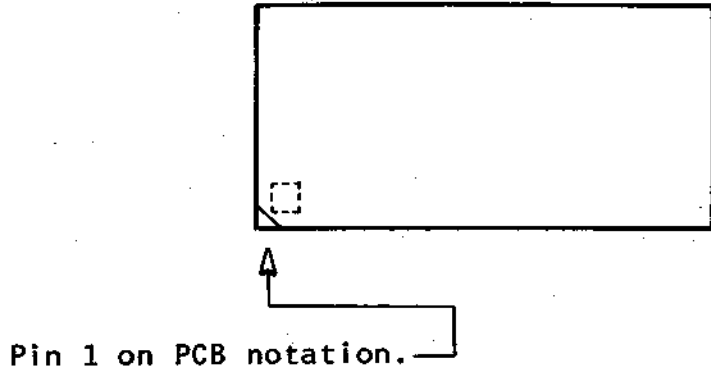


Fig. 1b Typical orientation marks viewed from above, pins facing away from you. Pin 1 is the top left hand corner in each case.

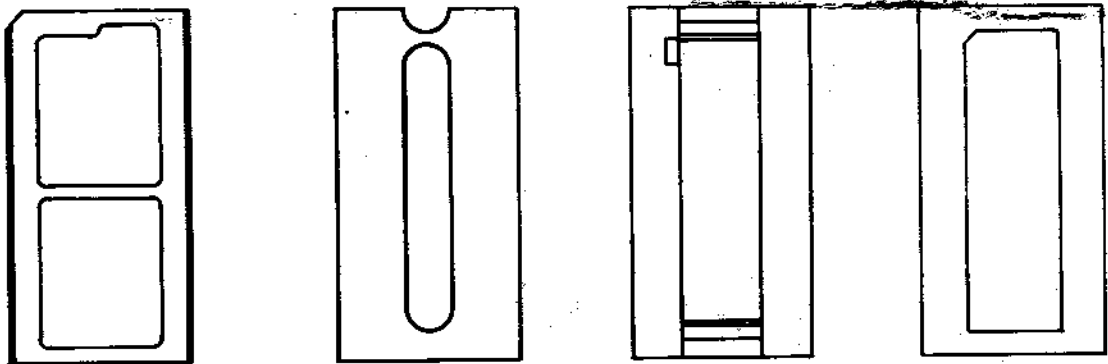
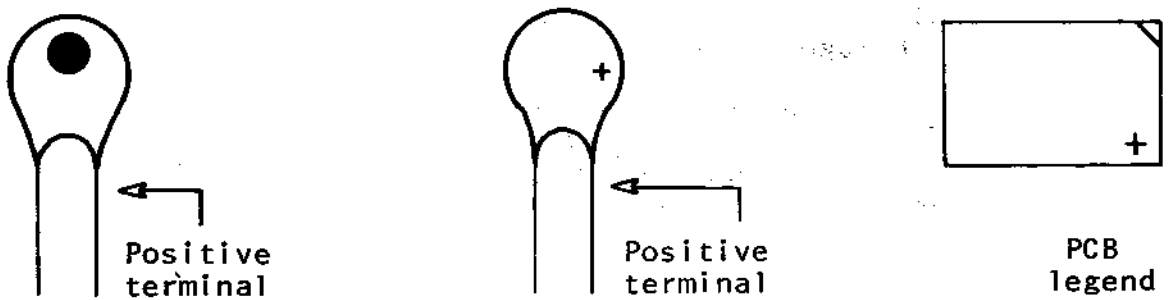


Fig. 2 Tantalum Capacitors.

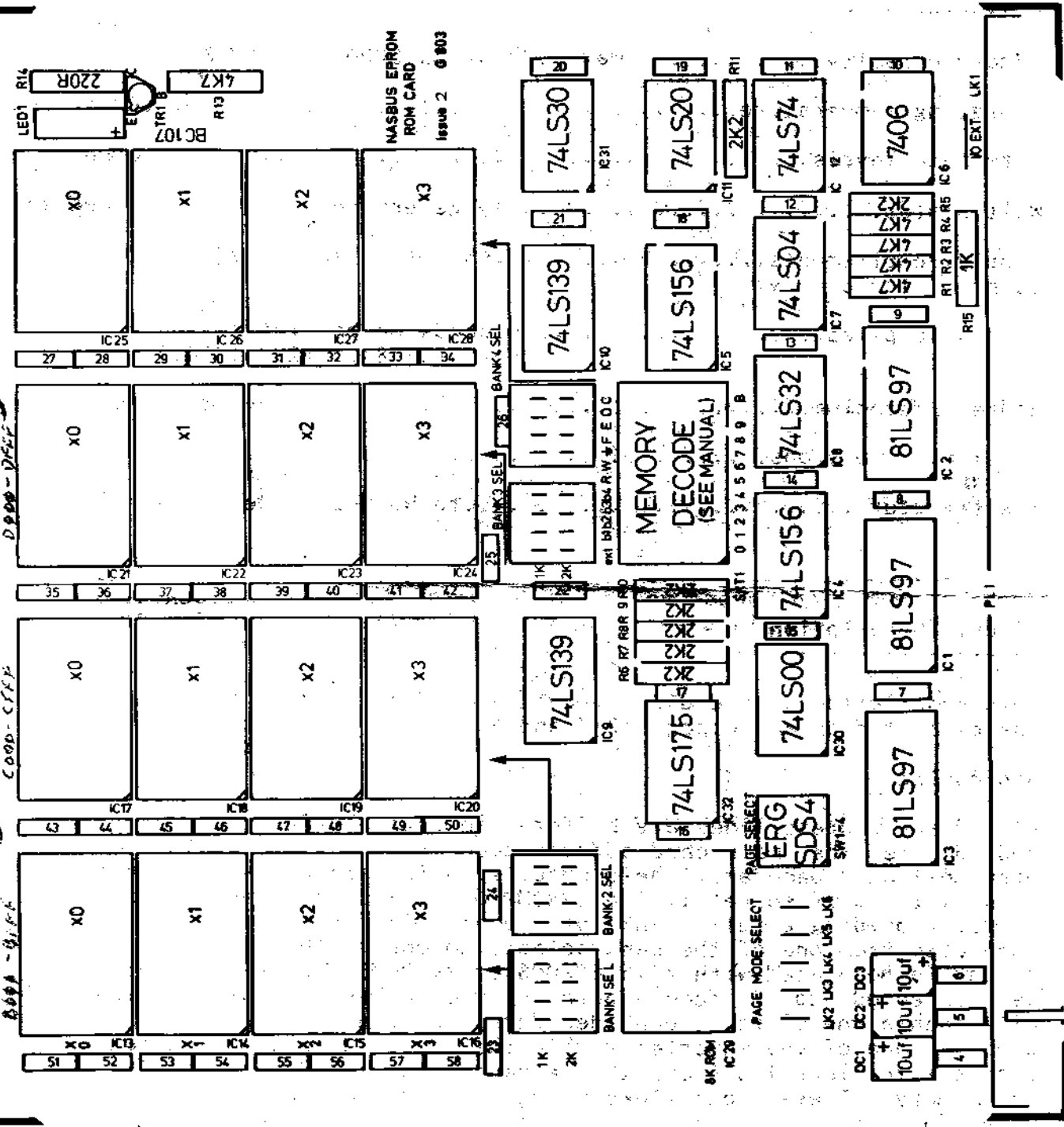


BANK ONE

BANK TWO

BANK THREE

BANK FOUR



64  
40  
3  
112

## Specifications

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Memory capacity.....max. 32k bytes EPROM or ROM & 8k bytes ROM

Operating temperature.....0C to 50C

Interface levels.....TTL compatible

Wait states.....only generated when card is accessed

Supply requirements.....+5v +/- 10% @ 250 mA typically  
(control logic only)

Memory supplies.....Depends on population and type used  
-5v (2708), +12v (2708) and +5v

Address decoding.....to any Z80 4k boundary

Physical dimensions.....8ins x 8ins

Bus structure.....to Nasbus Issue 4 specification

## Circuit Description

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This description of the G803 circuit should be read in conjunction with the circuit diagram on pages 2-7 and 2-8.

### Addressing

All of the address lines are buffered in octal buffers IC 1 and 2. IC 4 and 5 are the main card address decoders. They are dual 2 to 4 line open collector decoders. Their outputs, which are active low, appear at pins 1 to 16 of socket 1. The EPROM/ROM bank selects appear at pins 20 to 23. Providing a full bank of memory is used, a link will be connected from one of the bank selects to one of the decode outputs. If a bank is populated with 2716 EPROMS or 2k ROMS then a bank select will be connected to 2 decode outputs. When a bank select goes low, this will enable one of the 4 bank decoders, ICs 9 and 10, which in turn enables one of the memories within the selected bank. By selecting the appropriate links ICs 9 and 10 are capable of decoding 1 or 2k blocks of memory. These four links blocks appear near the memory array. The other functions of these links is to select +12v and -5v for 2708 EPROMS. When a bank is selected, the output of IC 8a becomes high. Also when MREQ, RD and page selecte are active, the output of IC 11a goes low enabling the output data buffer IC 3 and activates the wait state generator (IC 12).providing it has been enabled.



### Wait States and M.EXT

To disable the wait state generator, connect a link between pins 18 and 17 of SKT 1. The 8k ROM is selected by connecting a link from pin 19 of SKT 1 to two of the 16 decode pins. If the Nascom 8k Basic ROM is to be used then link pin 19 to pins 15 and 16 of SKT 1. The Basic will then reside at its normal address of E000H to FFFFH. A noticeable increase in Basic execution times can be achieved by removing the ROM from Nascom 2 and installing it in this card, because Wait states will only be generated when the card is accessed. However do not forget to turn off the Wait state generator on Nascom 2, and remove the BROM link on the header plug (8 to 9). If no other cards in the system are providing the M. EXT signal, then connect a link between pins 24 and 1 of SKT 1. Please note that this signal is only required for Nascom 1.

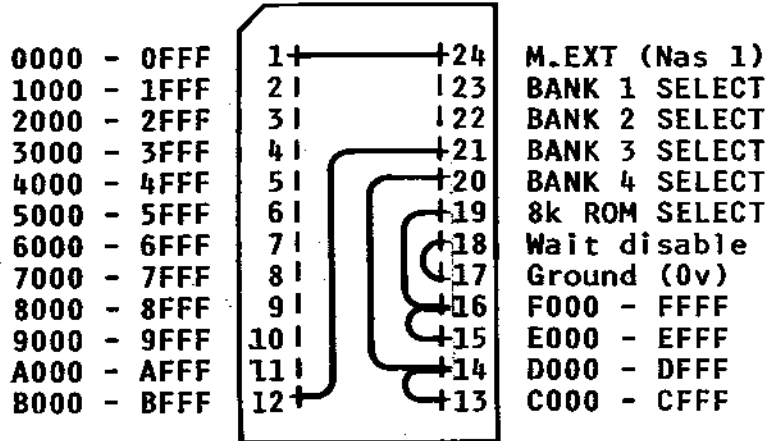
### Page Mode and I/O EXT

The page mode circuitry is fully compatible with the page mode facility used on Nascom's RAM B cards. This system of paging allows up to four memory cards to be used within the system. Upon reset, page 0 is automatically enabled; therefore any card residing in page 0 will be brought into the system address space. The reset signal causes the four non-inverted outputs of IC 32 to go low. These signals are taken to the DIL switch block where one switch will be used to select the page that the EPROM card will reside in. As the page mode enable signal is active high, it is necessary to make page 0 high on power-up. When reset occurs, IC 30a and b (RS flip-flop) provides a high output to IC 8d which is gated with the page 0 output of IC 32. The combination of input signals on IC 8a forces its output to go high. This output is the page 0 output which is connected to the first page mode switch. When a different page is selected, by writing data to port FFH, the output of the flip-flop becomes low which in turn allows normal selection of page 0 by software thereafter. IC 30 decodes port FF. When the bus signals WR and IORQ are active and providing IC 30's output is active (low), data will be clocked into the quad D type flip-flop IC 32. Unlike the Nascom RAM card, only four data lines are required as no page write signals are required for this card. When the card is paged in the LED will light up. The I/O EXT link on the card is in fact a return of the address line A7. When an address from 00H to 7FH is requested this line is low, which enables the Nascom to function normally. This partial decode is also used on the RAM B card. Please note that only one card in the system should be used to provide this signal

007F

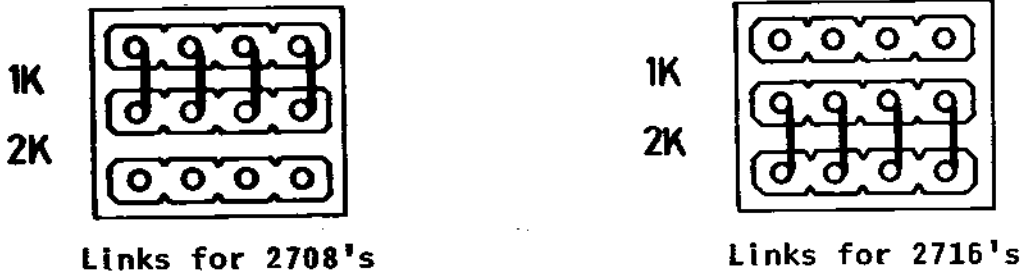
0111111

Fig. 4 Address decodes SKT 1



The link arrangement in Fig. 4 Shows (1) Nascom 1 residing at 0000H to 0FFFH, (2) Banks 1 and 2 unused, (3) Bank 3 with 2708's installed residing at B000H to BFFFH, (4) Bank 4 with 2716's installed residing at C000H to DFFFH, (5) The 8k "Basic" ROM residing at E000H to FFFFH and the Wait state generator is disabled.

Fig. 5 Power and Bank Decodes.



Using "Page Mode"

When standard Page mode operation is required LK6 should be installed and the page at which the card will reside is then chosen moving one of the four DIL switches. Remember that page 0 is always active upon power-up and system reset. When the card is selected by software the green LED will illuminate.

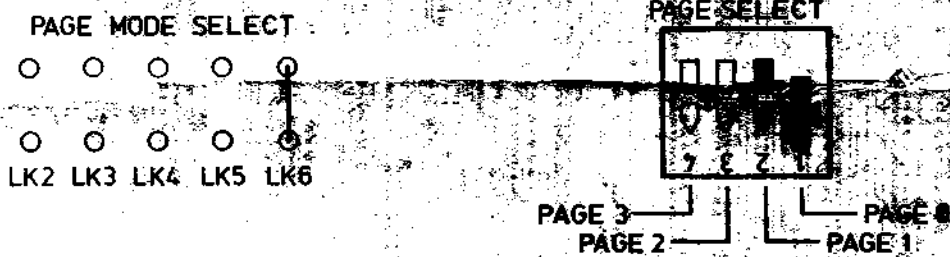
To control the paging system it is necessary to write data to Port FFH. Bit 1 is page 0, Bit 2 is page 1, Bit 3 is page 2 and Bit 4 is page 3. Bit 1 is the least significant bit. The control bit is logical 1 to enable a card. The bit arrangement is common in sequence to the Nascom

RAM B card. Bit's 5 to 8 are only used on RAM B cards and they are the page mode write enable bits (logical 1 to activate a card). Bit 5 is the least significant write enable bit.

If the page mode facility is not required only LK5 need be installed. LK2, 3 and 4 are provided for extended page mode. These links are connected to the system Bus lines 46, 47 and 48. They may also be used to provide remote page switching.

The page mode facility is useful when maximum program speed is required and the program is situated in slow memory (EPROM etc). By using the page mode facility it is possible to transfer the contents of the EPROM into Dynamic RAM, switch off the EPROM card and then run the program at 4Mhz without wait states. There is a marked improvement when running a "Basic" program. The other advantages of page mode are that more than 64k of memory can be used in the system and all firmware can reside in the system all of the time.

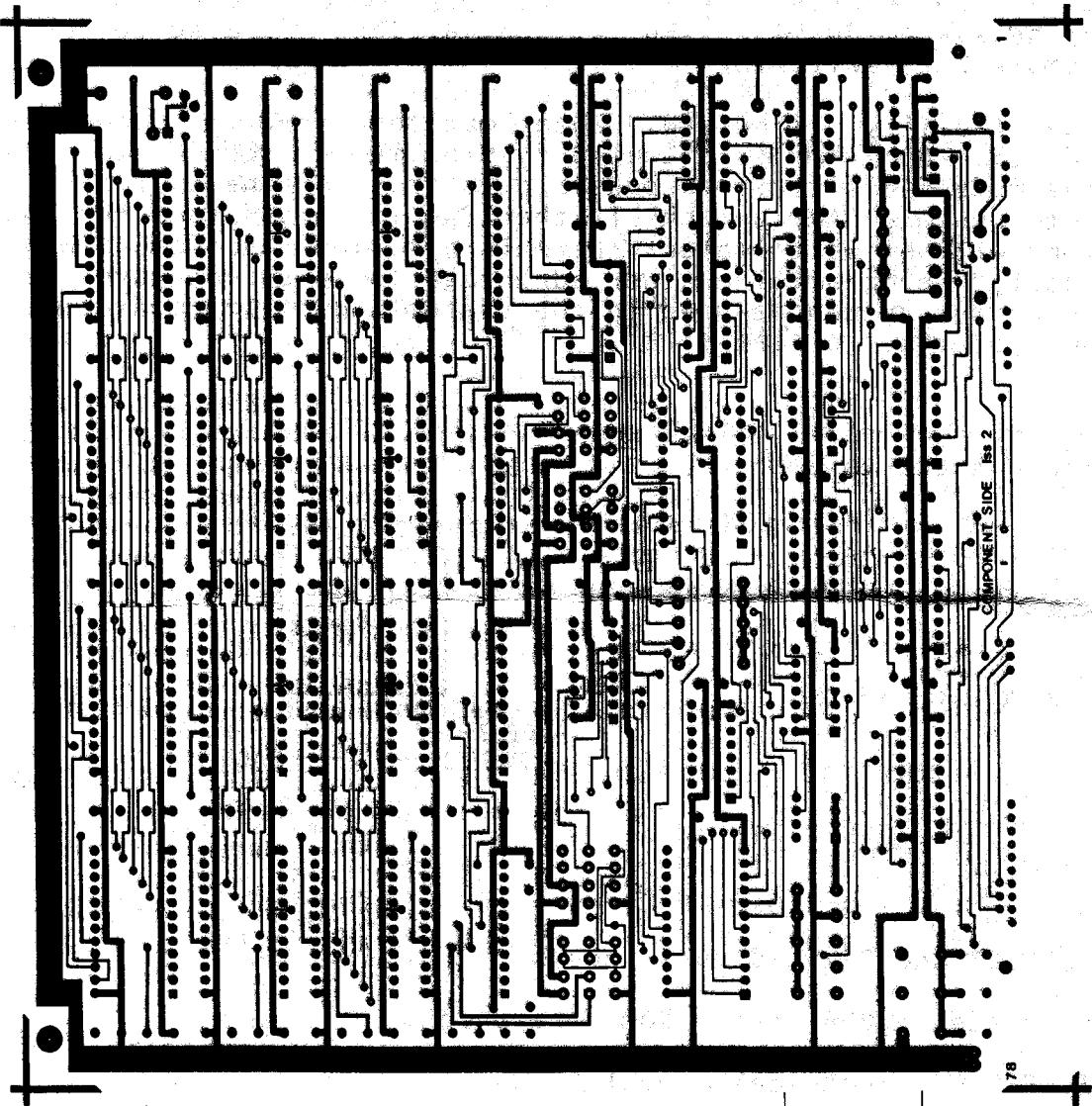
Fig. 6 SW1 to 4 & LK2 to 6



#### References

1. 2708 and 2716 IC data sheets
2. Mostek 36000 series ROM data sheet
3. Z80 CPU Technical manual
4. Nascom 1 and 2 constructional notes
5. Nascom Buffer card specification
6. Nasbus functional specification. Issue 4

This documentation was prepared on the NAS-PEN Text processor.



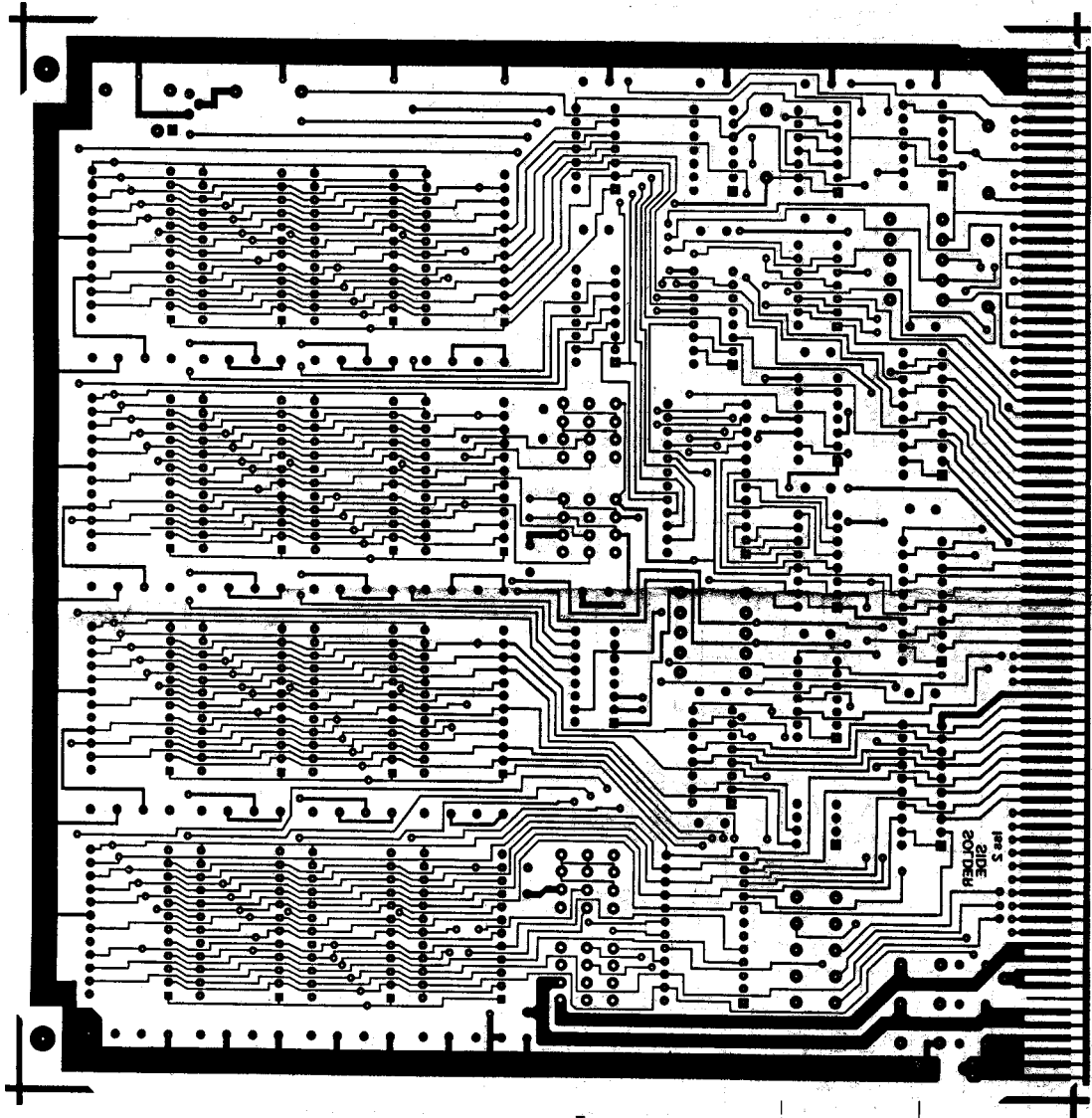
FINISHED HOLE SIZE IN MM

- 0.60
- 0.80
- 1.00
- 1.20
- 2.0

MASBUS EPROM/ROM  
CARD

5-6-80

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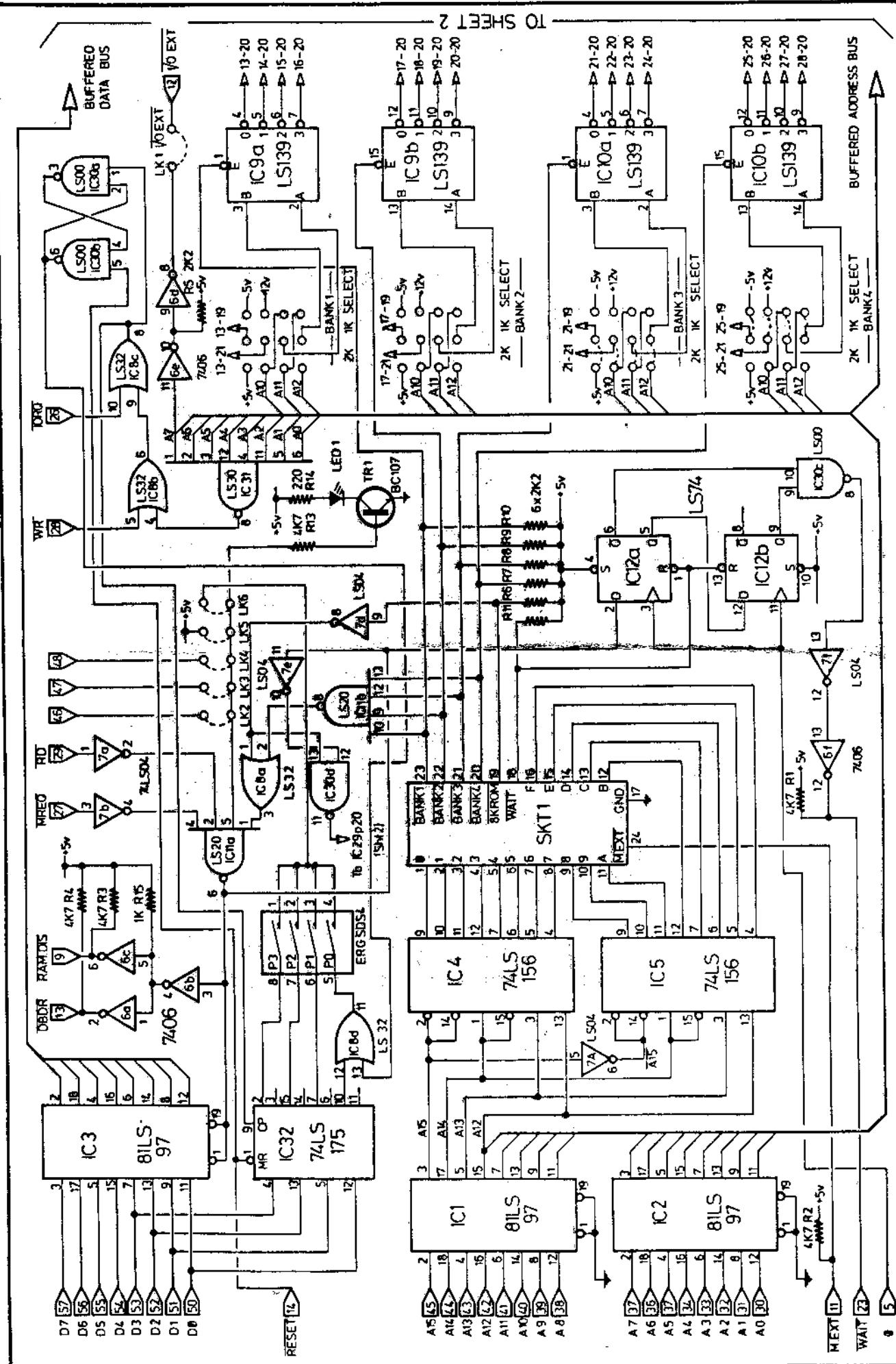
FINISHED HOLE SIZE IN MM

- 0.60
- 0.80
- 1.00
- 1.20
- 2.0

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CARD

6-6-80

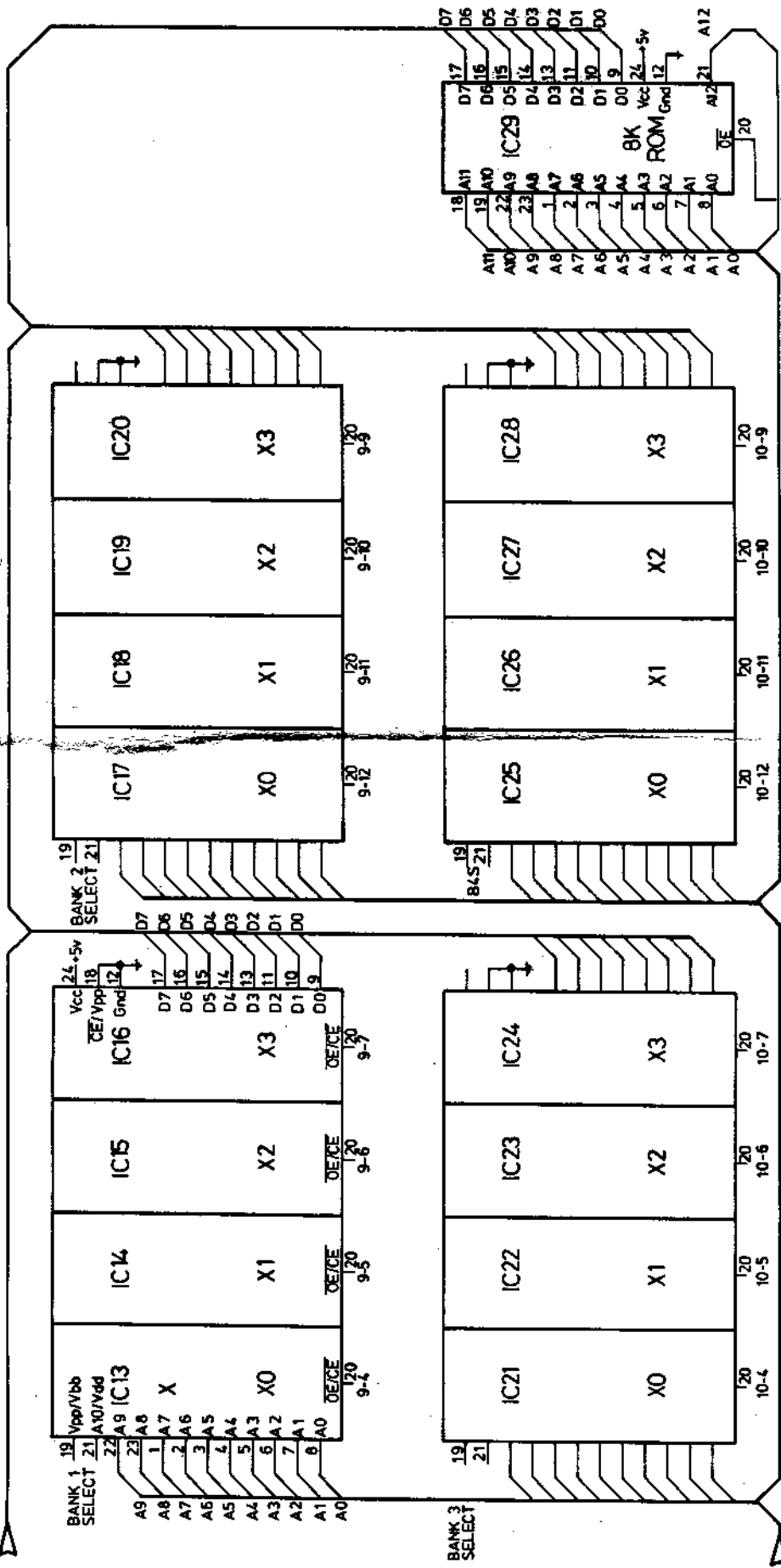
FRONT  
SIDE



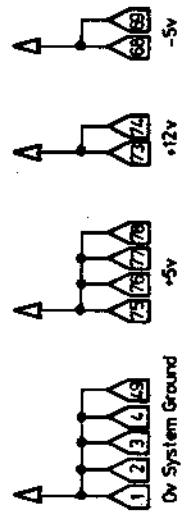
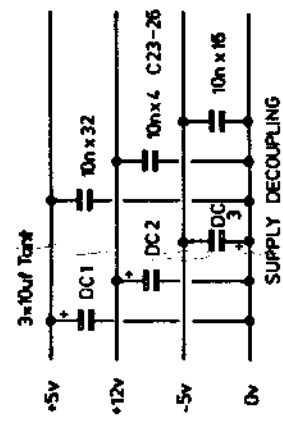
Issue 2 Sheet 1 of 2 Drawn NB  
 Date 19-5-80 Drawing No  
 Revisions:-

# NASPROM EPROM/ROM CARD

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From IC30pin (SM1)



Issue 2 Sheet 2 of 2 Drawn NB  
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