The Gemini MultiBoard Microsystem

'RAM 64'

80-BUS
64K DYNAMIC RAM CARD

INSTRUCTION MANUAL
AND
FUNCTIONAL DESCRIPTION

G802
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Introduction

The Gemini G802 'RAM64' is a dynamic random access memory board that is both 80-BUS and Nasbus compatible, allowing it to be used with both Gemini Multiboard and Nascom systems. The board is configured to have a memory capacity of 64K bytes of user RAM, allowing the total memory capacity of the Z80 to be implemented on a single card. This is made possible by the use of thirty-two 4116 (16,384x1 MOS dynamic RAM) memories. 'RAM64' also includes logic for a page mode operation which, when used with the appropriate software, permits upto four fully populated Gemini G802 'RAM64' and G803 'EPROM/ROM' boards to be fitted in one system.

This manual contains all of the information necessary to operate your 4MHz, 64K dynamic RAM card.

Guarantee

Your Gemini G802 'RAM64' board is guaranteed by the supplier (your Distributor) for one year from the date of purchase. However, being a system module, any faults attributable to the incorrect implementation of the board within your system will be fully chargeable as to both parts and labour. The guarantee extends as far as the original hardware as supplied and no work on 'RAM64s' modified in any way will be carried out.

Any queries regarding the implementation and operation of your 'RAM64' should be directed at your Gemini distributor.

Installing `RAM64'

Link Options.

There are four links on `RAM64' which should be set according to the specific requirements of your system. If the system is a Gemini Multiboard System, then no alterations are required to the links as set during manufacture. Further details of the link functions are given in Section 3.

LK1 Link `ON' to enable page mode circuitry
Link `OFF' to disable page mode circuitry

LK2 As LK1

LK3 ONLY required with Nascom 1. If normal Nascom operation required link `0'. If CP/M operation required then link `F'. Omit link if not an N1. N.B. There must be NO link on SKT1 to the same address block as the N1.

LK4 Fitted ONLY if ALL of the following conditions apply:
(a) Page mode option required
AND (b) Card is to be used with Nascom 1 or 2
AND (c) NO other card (e.g. Nascom I/O board, RAM B, EPROM/ROM board or another `RAM64') is providing an IOEXT or NASIO signal.

Page Mode

`RAM64' contains a page mode facility that allows the board to be enabled or disabled under software control. The facility allows upto four page mode cards to be operated on a single system, and the Read and Write circuitry of each card may be enabled independantly, allowing data transfer to take place between the different cards.

The `Page' of each card is determined by the position of the DIL switch on the card (labelled `PG SELECT'). The card selected as `Page 0' (switch towards the edge connector) is the card that will be enabled (both Read and Write) following power-on or a Reset.

Selection between cards is achieved by writing data to Z80 Port FF. The least significant nibble of the byte written to this port determines which card is to be enabled for Z80 Read cycles and the most significant nibble determines the card selected for Z80 Write cycles. The least significant bit of each nibble selects the card designated as `Page 0'. Note that with this method of selection it is possible to enable more than one card for either function. It is permissable to enable the Write function of more than one card, but if more than one card is enabled for Read then the resulting data clashes will probably cause loss of control of the system.

Examples of Page selection:

Byte output to port FF	Boards selected
11 or Reset	Page 0 Write and Read
21	Page 1 Write, Page 0 Read
F2	All Pages Write, Page 1 Read
88	Page 3 Read and Write

SECTION 2
=========

MEMORY TEST PROGRAM.

This program is designed to run under Nas-Sys on a Nascom 1 or 2. With a Gemini Multiboard System running RP/M the memory is tested automatically following Reset. The program is split into two halves, part 1 executes three tests giving the following error letter if the condition is not met:-

A - Location not set to zero
B - Walking bit test
C - Location not set to FF

Part two of the program loads a jump instruction into each location and then executes it, moving the jump through the memory as it goes. If the program "Crashes" because of a fault in memory the screen will hold the last address, or if this is cleared or corrupted locations 0D49 & 0D4A will still contain it. The program will loop till a system reset or fault occurs.

Execute 0C80 ssss eeee. Where ssss is the first location and eeee is the last location of memory to be tested.

```
0C80 EF 0C 00 EF 4D 45 4D 4F 52 59 20 54 45 53 54 20
0C90 50 41 52 54 20 31 0D 00 2A 10 0C AF ED 5B 0E 0C
0CA0 ED 52 E5 44 4D 2A 0E 0C E5 54 5D 13 36 00 ED B0
0CB0 E1 C1 16 00 AF BE 3E 41 C4 3A 0D 3E 01 77 BE F5
0CC0 3E 42 C4 3A 0D F1 20 03 17 30 F2 3E FF 77 BE 3E
0CD0 43 C4 3A 0D 7A B7 C4 47 0D 23 0B 78 B1 20 D3 EF
0CE0 50 41 52 54 20 32 20 20 4F 50 2D 43 4F 44 45 20
0CF0 46 45 54 43 48 20 54 45 53 54 0D 00 2A 10 0C AF
0D00 ED 5B 0E 0C ED 52 44 4D 0B 0B EB E5 3E C3 77 23
0D10 11 27 0D 73 23 72 E1 ED 5B 29 0C C5 DF 66 22 4A
0D20 0D ED 53 29 0C C1 E9 23 0B 78 B1 20 DE EF 4C 4F
0D30 4F 50 49 4E 47 0D 00 C3 83 0C F5 F7 DF 69 C5 DF
0D40 66 C1 DF 69 14 F1 C9 DF 6A C9 00 00 00 00 00 00
```

Upon execution of the above program the VDU should output the following message if the Memory card is functioning correctly.

```
MEMORY TEST PART 1
PART TWO OPCODE FETCH TEST
LOOPING
```

This message will be repeated until either a fault condition arises or a system reset is performed. However if the `RAM64' is faulty the VDU would output a message similar to the example below:-

```
MEMORY TEST PART 1

A aaaa   B bbbb  C cccc
A aaaa
A aaaa   B bbbb

PART 2  OPCODE FETCH TEST
eeee
```

Where aaaa is a location in memory that will not set to zero, bbbb will not accept certain data patterns, cccc will not set all bits high and eeee was the last address that did not accept a jump command.

SECTION 3

SPECIFICATION

Memory capacity	64K bytes
Memory cycle time (without wait state)	400ns min.
Memory access time (without wait state)	150ns max.
Operating temperature	0C to 50C
Interface levels	TTL compatible
Supply requirements	+12V +/- 5% @ 170mA typ.
(fully populated)	+5v +/- 5% @ 350mA typ.
	-5v +/- 5% @ 30mA typ.
Physical dimensions	8 x 8 inches.

Circuit Description

The following circuit description should be read in conjunction with the circuit diagrams.

ADDRESS and DECODE LOGIC. Address lines A0 to A11 are buffered by ICs 50 and 51. Buffered address lines A0 to A13 are routed to address switches IC42 and 52, where they are switched into the memory array to provide row (A0 to A6) and column (A7 to A13) addresses. The row and column addresses are strobed into the memory by two negative going clocks called Row address strobe (RAS) and column address strobe (CAS). By the use of RAS and CAS the address bits are latched into the memory for access to the required memory location. Because the Z80 CPU does not guarantee that the address bus will hold valid information past the rising edge of MREQ on an op-code fetch, A12 to A15 are latched (IC49) each time MREQ is active. This prevents glitches appearing on the RAS lines. A12 to A15 are decoded in ICs 32 and 33 to provide select signals for each 4K byte block of memory starting at any 4K boundary. These signals arrive at pins 1 to 16 of SKT1. Link LK1 provides the NASMEM signal which is necessary to decode the internal addressing of Nascom 1. This signal is not required by Nascom 2. Pins 17, 18, 19 and 20 of SKT1 are the memory array bank selects. These selects should be commoned to four of the 16 4K decodes. A0 to A7 are also routed to IC53 for Port decoding when "Page-mode" is used.

MEMORY CONTROL LOGIC. MREQ is buffered by IC 51 and inverted by IC20. The output from IC20 is inverted and then ORed with the output from the 4MHz Z80 precharge extender circuit (IC21). The RAS signal is then ORed in IC9 with the ANDed bank decode and Refresh signals. When a memory bank is decoded only one RAS line to the memory array goes low. However, if a memory refresh is being performed, all the RAS inputs to the array will go low. The active delay line (IC31), whose input is MREQ, goes low at pin 4 approximately 60ns after MREQ goes active. All memory timing is referenced to MREQ. The 60ns delay was chosen to allow an adequate margin for the row address hold time. The signal controls the address multiplexers (IC42 and 52). Until now the memory array has been receiving the row addresses (A0 to A6). When MUX goes low the column addresses (A7 to A13) are then switched to the array address inputs. After a further delay of approximately 30ns the delay line goes low at Pin 11 (CAS). This signal is then ORed in IC11 with Refresh. If a refresh is not being performed the memory array will receive CAS. It is necessary to delay CAS from MUX in order to allow the addresses to stabilise after being switched. Whe CAS is received the memory then latches the column addresses.

READ and WRITE LOGIC. The Write signal is buffered in IC51 and is then ORed with the output of the card page mode write enable circuitry (if fitted). If page mode is not installed then LK2 should be connected to 0V. This will permanently enable write enable. However, if page mode is installed, this link should be connected the other way round. This connects the write enable signal to the page mode circuitry and only when the card is paged in will this be enabled. The combined Write and write enable signal is then taken to the memory array WR input via a 33R resistor. The RD input is buffered in IC20 which appears at an input of IC22. The other inputs to this gate are MREQ, memory decode and RAMDIS. The output of the gate when active and when page read enable is active enables the data output buffer (IC43) and will bring DBDR low via IC20 and TR1. The memory will output data when addressed only when its write inputs are not active. The card read enable signal is similar to the previously mentioned write enable signal. When page mode is not installed, it is necessary to link LK1 to 'OFF'.

PAGE MODE upgrade kit. IC53 decodes the port (port FF) and is ORed with WR in IC47. This signal is subsequently ORed with IORQ which is used as a clock to latch data into IC45. The outputs from IC45 will all be low on power-up as the system reset is connected to the master reset input of this IC. Also on power-up, IC48 pin 6 will be high bringing IC47/3 and 6 high. A four position DIL switch selects the card page number. If in position 0 as marked on the PCB, the card will become active on power-up and up until such time as the port status changes. By changing the data of port FF one card can be paged out and another paged into the system. Because of this method of paging it is possible to enable one card to read only and another to write only; so by allowing the processor to read and write to the same address, data will be transferred from one page to another. This illustrates only one of many ways in which the page mode facility can be used. Address line 7 provides a NASIO signal when link LK4 is fitted. This is only a partial decode and needs only be used when page mode is required AND a Nascom 1 or 2 is in use AND no other card is providing the NASIO signal.

LINKS

Links 1 and 2

Links 1 and 2 are set according to whether or not the page mode option is fitted. Link 1 is in the read circuitry and should be set to the 'OFF' position if the page mode option is not fitted. Link 2 is in the write circuitry and should be set similarly.

Link 3

Link 3 is only applicable to Nascom 1 systems. This link is used to provide a 4K block decode back to the Nascom 1. The memory internal/external link on the Nascom 1 should be set to external. If normal Nascom 1 operation is required then Link 3 should be set to '0'. If, for example, a CP/M disk system is in use, and it requires the Nascom 1 4K block to be located from F000 to FFFF, then Link 3 should be set to 'F'. If it is required to set the Nascom 1 to any other 4K block then a wire link should be inserted from the common of Link 3 to the relevant pin on SKT1.

PLEASE NOTE: Whichever 4K block is chosen for the Nascom 1, there must be NO link connection for any dynamic RAM made to the corresponding 4K select pin on SKT1.

Link 4

Link 4 is ONLY required when ALL of the conditions specified in paragraph 8 on page 1-4 are true. This link feeds buffered address line 7 back onto the bus on the NASIO line (12). The port addressing internal/external switch (LSW2/8) on the Nascom 2 should be set to EXT (up). This signal then acts as a partial decode for the Nascom 2 on board ports or external page mode port.

APPENDIX - ADDRESSING LINK OPTIONS
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The addressing of each of the four 16K blocks of memory is determined by connecting four of the 4K decodes to each of the BANK pins.

It does not matter if any of the RAM blocks overlap any memory on the Nascom 1, 2, Gemini G811 CPU board or Gemini G803 EPROM board as these boards will generate a RAM disable (RAMDIS) signal, overiding the memory on the `RAM64' board.

Signals on SK1

0000-0FFF	1	20 BANK 0 (ICs 1 to 8)
1000-1FFF	2	19 BANK 1 (ICs 12 to 19)
2000-2FFF	3	18 BANK 2 (ICs 23 to 30)
3000-3FFF	4	17 BANK 3 (ICs 34 to 41)
4000-4FFF	5	16 F000-FFFF
5000-5FFF	6	15 E000-EFFF
6000-6FFF	7	14 D000-DFFF
7000-7FFF	8	13 C000-CFFF
8000-8FFF	9	12 B000-BFFF
9000-9FFF	10	11 A000-AFFF

Suggested link options

64K of Memory
0000H - FFFFH
Banks 0 - 3